nPM6001

Product Specification

v1.0

NORDIC® SEMICONDUCTOR

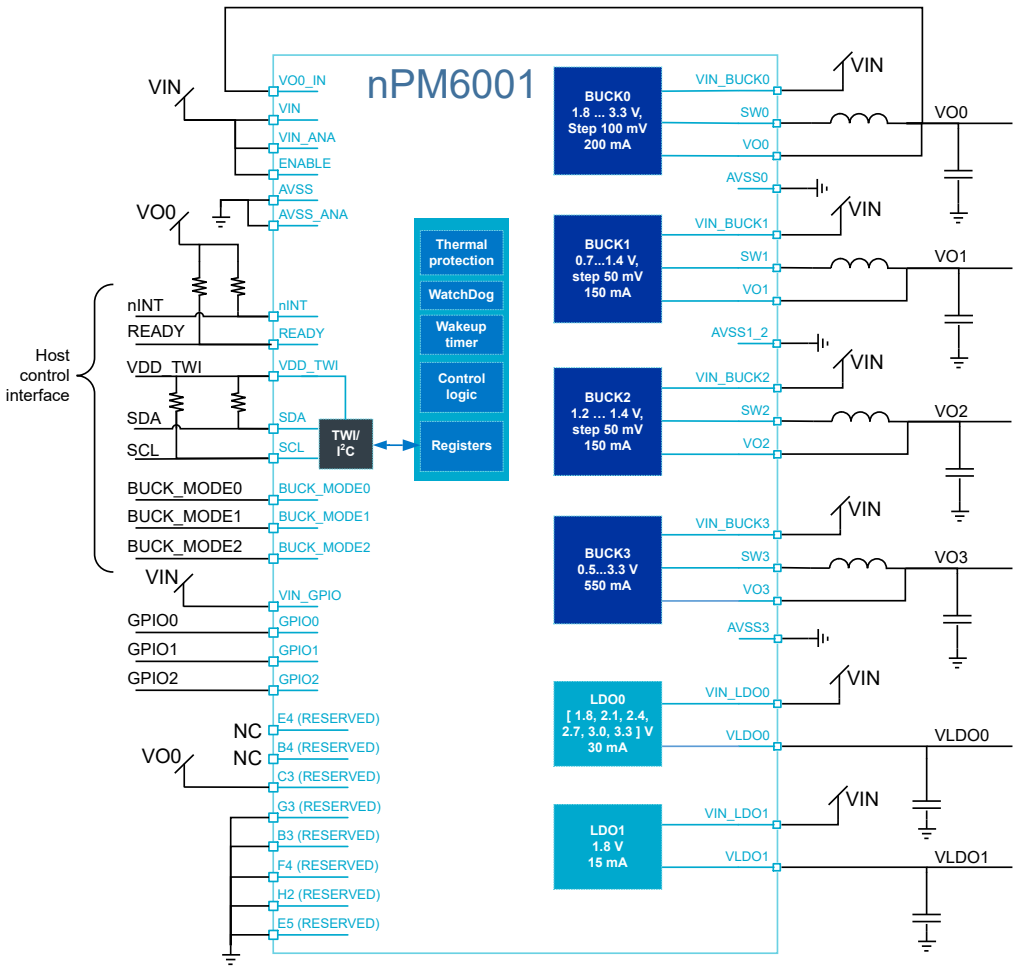
nPM6001

nPM6001 is an integrated Power Management IC (PMIC) with a low power standby mode that is optimized for battery powered applications. It has four highly efficient buck regulators with configurable dual-mode output and two low-dropout linear regulators.

Designed for space constrained applications, nPM6001 is an extremely compact device in a 2.2x3.6 mm WLCSP package.

Battery life is extended due to the low quiescent current (IQ) from the buck regulators when the device is in deep sleep. VIN consumes 1.2 µA of total quiescent current when BUCK0, BUCK1, and BUCK2 are running with no load current while maintaining the output voltages.

- Ultra-high efficiency extends battery life and reduces the battery footprint
- Small solution size leaves space for additional features without increasing product size
- Regulator output voltage levels configurable through the TWI interface
- Dedicated pins control buck regulators' operating modes between high and low current modes



Key features

Features:

- 3.0 V to 5.5 V operating input voltage range
- 1.2 µA typical operational quiescent current
- 1.8 V to 3.3 V, 30 mA, low-dropout linear regulator
  - Output programmable in 300 mV steps
- Fixed voltage, 1.8 V, 15 mA, low-dropout linear regulator
- Three general purpose I/Os
- Thermal protection
  - Thermal warning interrupt
  - Thermal shutdown protection
- On-chip watchdog
- Hibernation mode
  - Four second to two years timer wake-up
  - 200 nA stand-by consumption
- Four step-down DC/DC regulators with dedicated control pins for switching between PWM and hysteretic modes with up to 95% efficiency
  - 1.8 V to 3.3 V, 200 mA, step-down converter
    - Output programmable in 100 mV steps
  - 0.7 V to 1.4 V, 150 mA, step-down converter
    - Output programmable in 50 mV steps
  - 1.2 V to 1.4 V, 150 mA, step-down converter
    - Output programmable in 50 mV steps
  - 0.5 V to 3.3 V, 550 mA, step-down converter
    - Output programmable in 25 mV steps

Applications:

- Advanced wearables
  - Health/fitness sensor and monitoring devices
- Portable video devices
- Asset trackers
- Interactive entertainment devices
  - Remote controls
  - Gaming controllers

Contents

1 Revision history

Date	Version	Description
September 2022	1.0	First release

2 About this document

This document is organized into chapters that are based on the modules available in the IC.

2.1 Document status

The document status reflects the level of maturity of the document.

Document name	Description
Objective Product Specification (OPS)	Applies to document versions up to 1.0. This document contains target specifications for product development.
Product Specification (PS)	Applies to document versions 1.0 and higher. This document contains final product specifications. Nordic Semiconductor ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Table 1: Defined document names

2.2 Core component chapters

Every core component has a unique capitalized name or an abbreviation of its name, e.g. LDO, used for identification and reference. This name is used in chapter headings and references, and it will appear in the C-code header file to identify the component.

The core component instance name, which is different from the core component name, is constructed using the core component name followed by a numbered postfix, starting with 0, for example, LDO0. A postfix is normally only used if a core component can be instantiated more than once. The core component instance name is also used in the C-code header file to identify the core component instance.

The chapters describing core components may include the following information:

- A detailed functional description of the core component
- Register configuration for the core component
- Electrical specification tables, containing performance data which apply for the operating conditions described in Recommended operating conditions on page 13.

2.3 Register tables

Individual registers are described using register tables. These tables are built up of two sections. The first three colored rows describe the position and size of the different fields in the register. The following rows describe the fields in more detail.

2.3.1 Fields and values

The **Id (Field Id)** row specifies the bits that belong to the different fields in the register. If a field has enumerated values, then every value will be identified with a unique value id in the **Value Id** column.

A blank space means that the field is reserved and read as undefined, and it also must be written as `0` to secure forward compatibility. If a register is divided into more than one field, a unique field name is specified for each field in the **Field** column. The **Value Id** may be omitted in the single-bit bit fields when values can be substituted with a Boolean type enumerator range, e.g. true/false, disable(d)/enable(d), on/off, and so on.

Values are usually provided as decimal or hexadecimal. Hexadecimal values have a `0x` prefix, decimal values have no prefix.

The **Value** column can be populated in the following ways:

- Individual enumerated values, for example 1, 3, 9.
- Range of values, e.g. [0..4], indicating all values from and including 0 and 4.
- Implicit values. If no values are indicated in the **Value** column, all bit combinations are supported, or alternatively the field's translation and limitations are described in the text instead.

If two or more fields are closely related, the **Value Id**, **Value**, and **Description** may be omitted for all but the first field. Subsequent fields will indicate inheritance with '..'.

A feature marked **Deprecated** should not be used for new designs.

2.3.2 Permissions

Different fields in a register might have different access permissions enforced by hardware.

The access permission for each register field is documented in the **Access** column in the following ways:

Access	Description	Hardware behavior
RO	Read-only	Field can only be read. A write will be ignored.
WO	Write-only	Field can only be written. A read will return an undefined value.
RW	Read-write	Field can be read and written multiple times.
W1	Write-once	Field can only be written once per reset. Any subsequent write will be ignored. A read will return an undefined value.
RW1	Read-write-once	Field can be read multiple times, but only written once per reset. Any subsequent write will be ignored.
W1C	Write 1 to clear	Field can be read multiple times. Bits set to 1 clear (set to zero) the corresponding bit in the register. Bits set to 0 are ignored.
W1S	Write 1 to set	Field can be read multiple times. Bits set to 0 clear (set to zero) the corresponding bit in the register. Bits set to 1 are ignored.

Table 2: Register field permission schemes

3 Product overview

This chapter contains an overview of the main features found in nPM6001.

3.1 Block diagram

The block diagram illustrates the overall system.

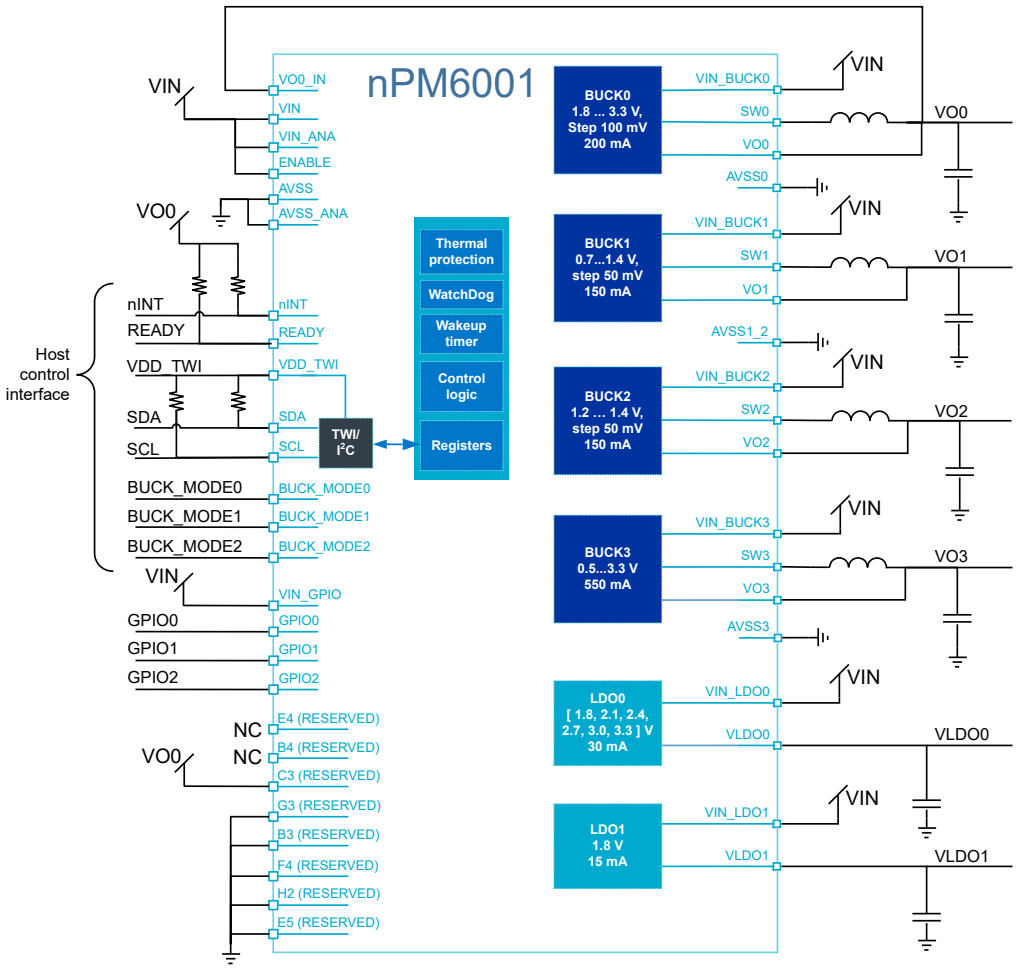


Figure 1: Block diagram

3.2 Key parameters

The key parameters are listed in the following table.

Parameter	Description	Notes	Min	Typ	Max	Unit
I_{ON}	Total quiescent current with no load	BUCK0, BUCK1 and BUCK2 running in hysteretic mode (BUCK3, LDO0 and LDO1 disabled). T = 25 °C VIN = 3.8 V		1.2		µA
I_{HIB}	Total current consumption from VIN in hibernate mode	VIN = 3.8 V T = 25 °C		200		nA
I_{OFF}	Total current consumption from VIN when ENABLE = 0	VIN = 3.8 V T = 25 °C		50		nA

Table 3: Key parameters

4 Absolute maximum ratings

Maximum ratings are the extreme limits to which the device can be exposed for a limited amount of time without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the device.

Pin	Note	Min.	Max.	Unit
VIN	Power **VIN**, **VIN_ANA**, **VIN_BUCK0**, **VIN_BUCK1**, **VIN_BUCK2**, **VIN_BUCK3**, **VIN_LDO0**, **VIN_LDO1**, **VO0_IN**, **VIN_GPIO**, **VDD_TWI**	-0.3	6.0	V
VSS	Power **AVSS**, **AVSS_ANA**, **AVSS0**, **AVSS1_2**, **AVSS3**		0	V
$VDIG_{I/O}$	Digital I/O **ENABLE**, **READY**, **SDA**, **SCL**, **nINT**, **GPIO0**, **GPIO1**, **GPIO2**, **BUCK_MODE0**, **BUCK_MODE1**, **BUCK_MODE2**	-0.3	6.0	V
$VANA_{I/O}$	Analog I/O **SW0**, **SW1**, **SW2**, **SW3**, **VO0**, **VO1**, **VO2**, **VO3**, **VLDO0**, **VLDO1**	-0.3	6.0	V
$V_{RESERVED}$	**RESERVED**	-0.3	6.0	V

Table 4: Pin voltage

	Note	Min.	Max.	Unit
Storage temperature		-40	+125	°C
MSL	Moisture Sensitivity Level		1	
ESD HBM	Human Body Model		1	kV
ESD CDM	Charged Device Model		750	V

Table 5: Environmental (WLCSP package)

5 Recommended operating conditions

The operating conditions are the physical parameters that the chip can operate within.

Symbol	Parameter	Min.	Nom.	Max.	Unit
VIN	Supply voltage **VIN**, **VIN_ANA**, **VIN_BUCK0**, **VIN_BUCK1**, **VIN_BUCK2**, **VIN_BUCK3**, **VIN_LDO0**, **VIN_LDO1**, **VIN_GPIO** The voltage levels for above pins must be within 100 mV from each other (including transients)	3.0		5.5	V
VO0_IN	**nINT** and **READY** supply voltage	1.71		3.6	V
VDD_TWI	TWI supply voltage VDD_TWI ≤ VIN	1.65		3.6	V
VO2	Supply voltage, custom configuration (BUCK2 unpopulated) VO2 ≤ VDD_TWI	1.14		3.6	V
VIN_{RAMP}	VIN supply ramp rate (R_{SOURCE} < 0.5 Ohm)	1			V/ms
T_J	Junction temperature	−40	25	125	°C
T_{OJ}	Operating junction temperature	−40	25	105	°C

Table 6: Supply voltages and temperature ranges

Pin	Parameter	Min.	Nom.	Max.	Unit
ENABLE		0		VIN	V
GPIO0, **GPIO1**, **GPIO2**	CMOS mode	0		VIN	V
	Schmitt trigger mode	0		VO2	
BUCK_MODE0, **BUCK_MODE1**, **BUCK_MODE2**	CMOS mode	0		VIN	V
	Schmitt trigger mode	0		VO2	
READY, **nINT**		0		VO0	V
SCL, **SDA**		0		VDD_TWI	V

Table 7: I/O voltage

Symbol	Parameter	Nom.	Unit
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	42	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	2	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	15.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	16	°C/W

Table 8: Dissipation ratings (JESD51-7)

5.1 WLCSP light sensitivity

WLCSP package is sensitive to visible and near infrared light, which means that a final product design must shield the chip properly.

6 POWER — Power supply

nPM6001 has six power rails that are controlled independently. Four of the power rails can be managed by highly efficient buck regulators. The two remaining power rails are managed by the LDO regulators.

The power supply is managed through TWI. BUCK[0..2] are partially controlled through TWI, meaning the output voltage and mode can be set using TWI, but they can not be switched on or off. BUCK3, LDO0, and LDO1 are fully controlled through TWI.

6.1 BUCK — Buck regulators

BUCK consists of four step-down regulators with the following features:

- High efficiency (low IQ) and low noise operation
- PWM and Hysteretic modes
- MODE control pin for setting PWM mode to minimize output voltage ripple

All **BUCK_MODE[n]** pins can be used to control any BUCK[n]. The buck regulators can be forced to PWM mode by setting bit SETFORCEPWM in register BUCK[n]CONF.PWM.MODE. PWM mode provides smaller output voltage ripple.

Pin control is enabled by setting bit SWREADY. BUCK[n] goes into Hysteretic mode when **BUCK_MODE[n]** is LOW. When **BUCK_MODE[n]** is HIGH, PWM mode is set.

The thermal sensor can be set to automatically turn on when BUCK[n] is running in PWM mode. To save power, the sensor is automatically switched off when all buck regulators are in Hysteretic mode.

BUCK[n] continues to run when an overcurrent is detected but its performance is reduced. When the current stabilizes, BUCK[n] resumes normal operation.

6.1.1 BUCK0

BUCK0 is an always-on buck regulator. It is running when VIN is above the Power-on reset threshold and **ENABLE** is HIGH.

The default output voltage for BUCK0 is 1.8 V. BUCK0 can supply load currents up to 200 mA in PWM mode and up to 30 mA in Hysteretic mode. The output voltage can be programmed in 100 mV steps between 1.8 V and 3.3 V and includes overcurrent detection. Output voltage settings for both PWM and Hysteretic mode must be identical.

The following are registers for BUCK0 output voltage programming:

Registers	Description
BUCK0.VOUT.ULP	Output voltage setting in hysteretic mode
BUCK0.VOUT.PWM	Output voltage setting in PWM mode
TASKS_UPDATE_VOUTPWM	Task for applying a new BUCK0VOUTPWM register value.

Table 9: BUCK0 output voltage

The (decimal) code for a given output voltage VO0 can be calculated using equation Code = (VO0 - 1.8 V) / 0.1 V.

To change output voltage while BUCK0 is running, BUCK0 must be set first to PWM mode before writing a new setting. This ensures a smooth voltage ramp. Hysteretic mode can be used again after a trigger task.

6.1.1.1 Electrical specification

Symbol	Description	Min.	Typ.	Max.	Units
VIN_{BUCK0}	Regulator input voltage	3.0		5.5	V
VO0	Regulator output voltage range	1.8		3.3	V
$VO0_{STEP}$	Output voltage programming step		100		mV
$VACC_{PWM}$	Output voltage accuracy Average voltage, not including ripple or transients PWM mode	-5		5	%
$VACC_{H}$	Output voltage accuracy Average voltage, not including ripple or transients Hysteretic mode	-5		5	%
VDO0	Drop out voltage (I_{OUT} = 100 mA)		350		mV
$VO0_{RIPPLE\_H}$	Output voltage peak-to-peak ripple in Hysteretic mode		50		mV
$VO0_{RIPPLE\_PWM}$	Output voltage peak-to-peak ripple in PWM mode over output current range			10	mV
I_{OUT_PWM}	Output current range, PWM mode	0		200	mA
I_{OUT_H}	Output current range, Hysteretic mode	0		30	mA
$LOAD_{TR}$	Load transient regulation, I_{OUT} rises or falls between 10 mA - 150 mA in 10 µs PWM mode	-50		50	mV
$LINE_{TR}$	Line transient regulation, VIN_{BUCK0} voltage rises or falls 300 mV in 10 µs with 1 kHz rate PWM mode		+/- 10		mV
EFF_{100MA}	BUCK efficiency with 100 mA load current VIN_{BUCK0} = 3.8 V, VO0 = 1.8 V, T = 25°C PWM mode		90		%

Table 10: BUCK0 electrical specification

6.1.1.2 Electrical characteristics

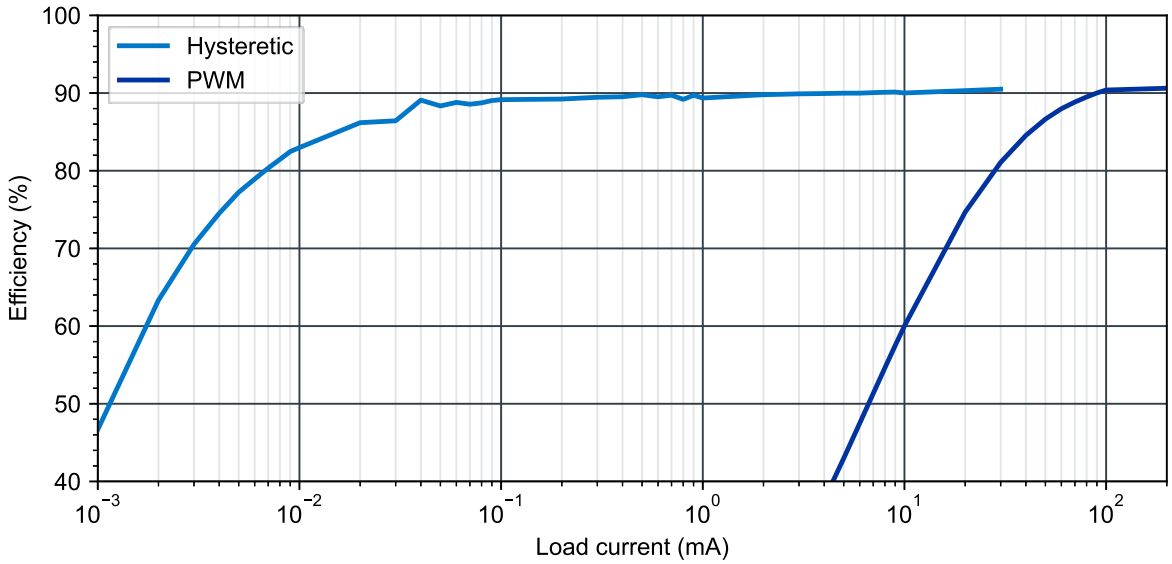


Figure 2: BUCK0 efficiency vs. load current (VIN_{BUCK0} = 3.8 V, VO0 = 1.8 V)

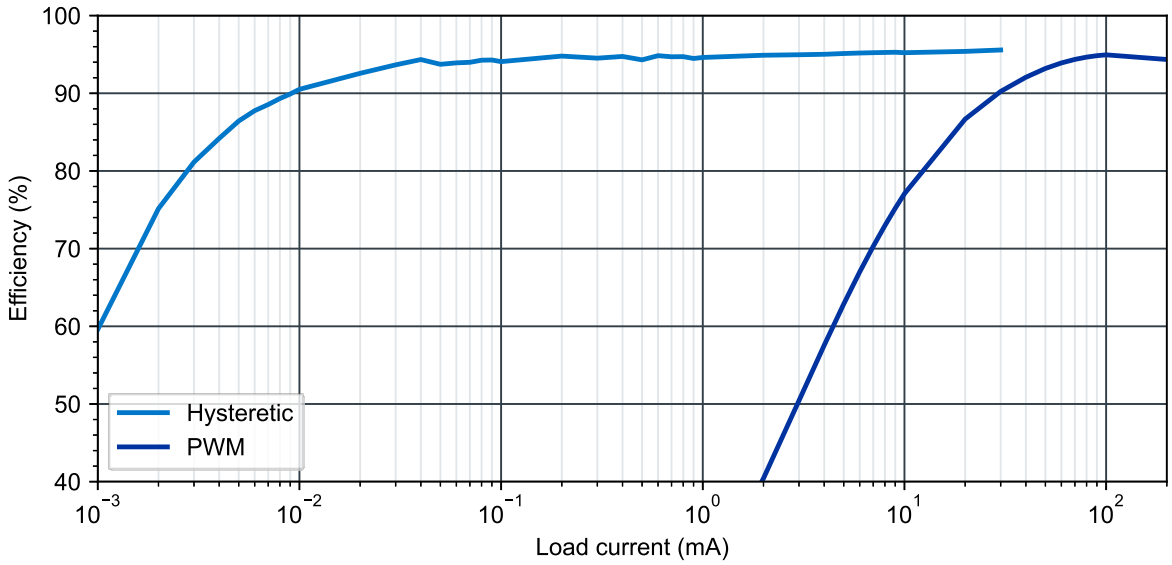


Figure 3: BUCK0 efficiency vs. load current (VIN_{BUCK0} = 3.8 V, VO0 = 3.3 V)

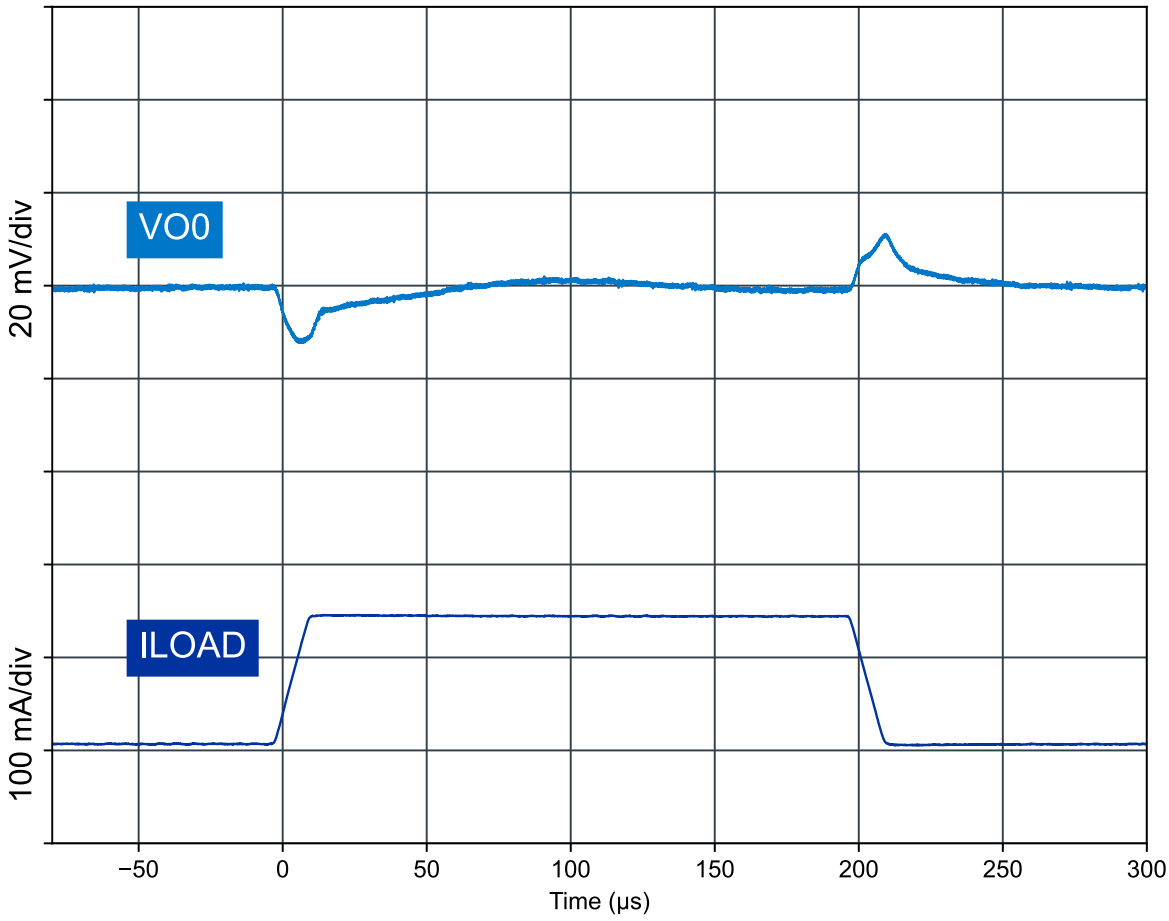


Figure 4: BUCK0 load transient (VIN_{BUCK0} = 3.8 V, VO0 = 1.8 V, I_{LOAD} 10 mA - 150 mA)

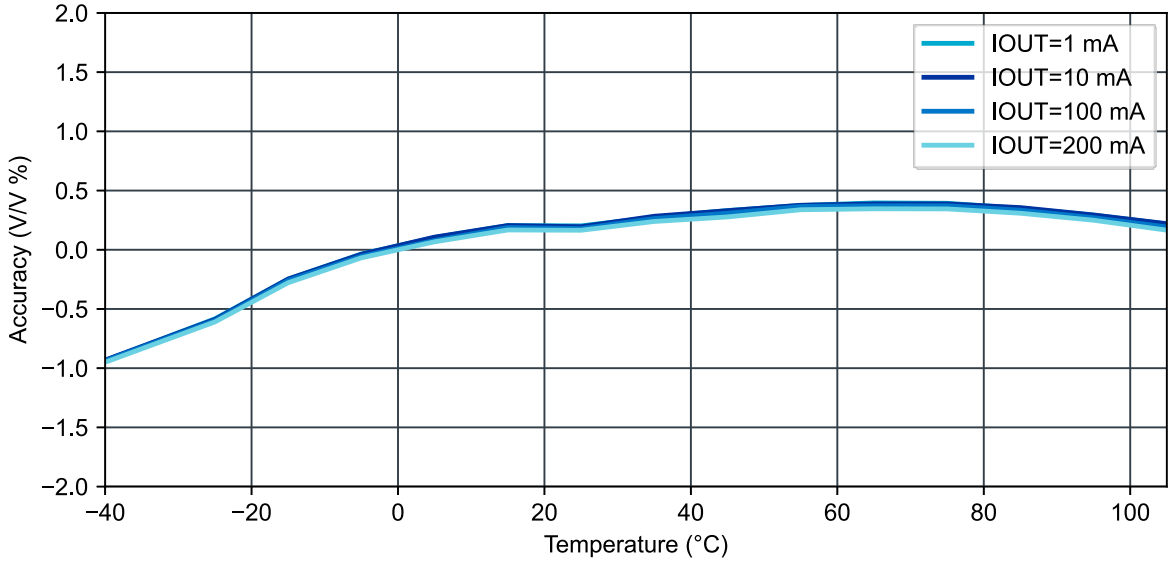


Figure 5: VO0 vs. temperature (VIN_{BUCK0} = 3.8 V, VO0 = 1.8 V)

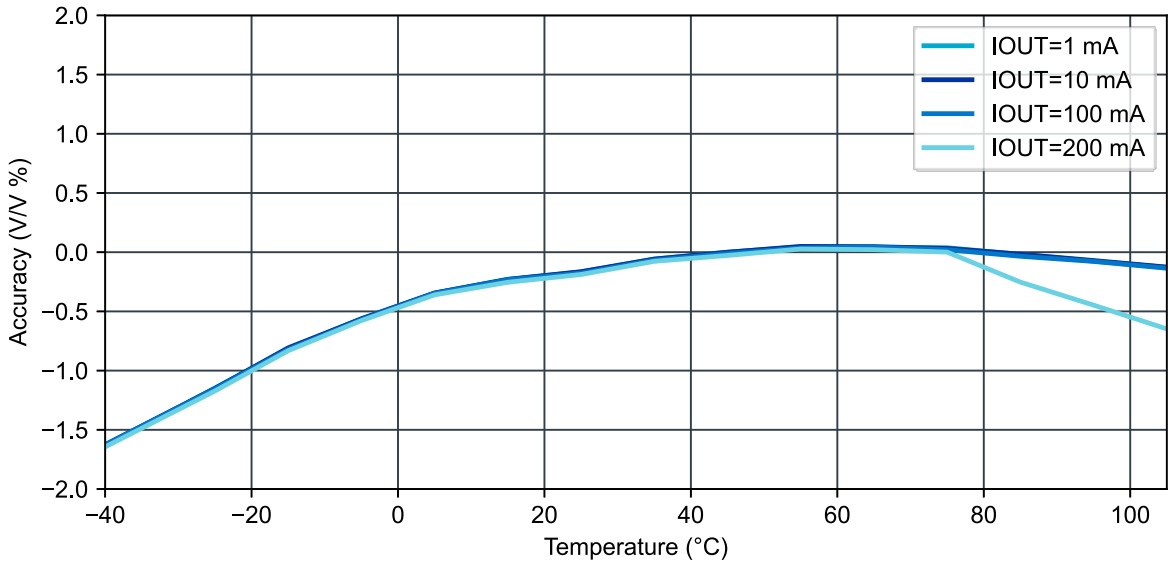


Figure 6: VO0 vs. temperature (VIN_{BUCK0} = 3.8 V, VO0 = 3.3 V)

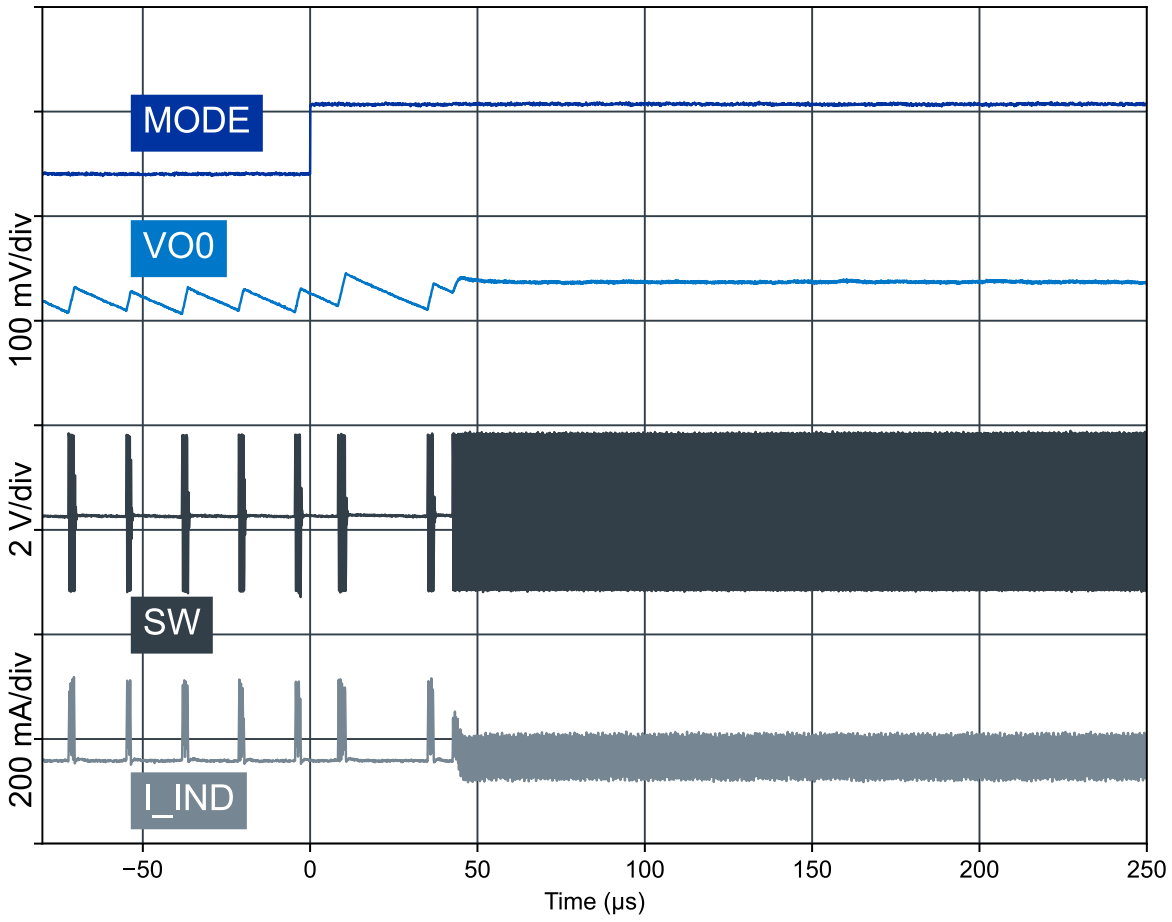


Figure 7: Mode transition from hysteretic to PWM (VIN_{BUCK0} = 3.8 V, VO0 = 1.8 V, I_OUT = 10 mA)

6.1.2 BUCK1

BUCK1 is an always-on buck regulator. It is running when VIN is above the Power-on reset threshold, **ENABLE** is HIGH, and the external components are present.

The default output voltage for BUCK1 is 0.8 V. BUCK1 can supply load currents up to 150 mA in PWM mode and up to 30 mA in Hysteretic mode. The output voltage can be programmed in 50 mV steps and must be between 0.7 V and 1.4 V. Output voltage settings for both PWM and Hysteretic mode must be identical.

The following registers are for BUCK1 output voltage programming:

Register	Description
BUCK1.VOUT.ULP	Output voltage setting in hysteretic mode
BUCK1.VOUT.PWM	Output voltage setting in PWM mode
TASKS_UPDATE_VOUTPWM	Task for applying a new BUCK1VOUTPWM register value.

Table 11: BUCK1 output voltage

The (decimal) code for a given output voltage VO1 can be calculated using equation Code = (VO1 - 0.7 V) / 0.05 V.

To change output voltage while BUCK1 is running, BUCK1 must be set first to PWM mode before writing a new setting. This ensures a smooth voltage ramp. Hysteretic mode can be used again after a trigger task.

6.1.2.1 Electrical specification

Symbol	Description	Min.	Typ.	Max.	Units
VIN_{BUCK1}	Regulator input voltage	3.0		5.5	V
VO1	Regulator output voltage range	0.7		1.4	V
$VO1_{STEP}$	Output voltage programming step		50		mV
$VACC_{PWM}$	Output voltage accuracy Average voltage, not including ripple or transients PWM mode	-5		5	%
$VACC_{H}$	Output voltage accuracy Average voltage, not including ripple or transients Hysteretic mode	-5		-5	%
I_{OUT_PWM}	Output current range, PWM mode	0		150	mA
I_{OUT_H}	Output current range, Hysteretic mode	0		30	mA
VO_{RIPPLE_H}	Output voltage peak-to-peak ripple in Hysteretic mode		50		mV
VO_{RIPPLE_PWM}	Output voltage peak-to-peak ripple in PWM mode			10	mV
$LOAD_{TR}$	Load transient regulation I_{OUT} rises or falls between 10 mA - 150 mA in 10 µs PWM mode	-50		50	mV
$LINE_{TR}$	Line transient regulation VIN_{BUCK1} voltage rises or falls 300 mV in 10 µs with 1 kHz rate PWM mode		+/- 10		mV
EFF_{100MA}	BUCK efficiency with 100 mA load current VIN_{BUCK1} = 3.8 V, VO1 = 0.8 V, T = 25°C PWM mode		84		%

Table 12: BUCK1 electrical specification

6.1.2.2 Electrical characteristics

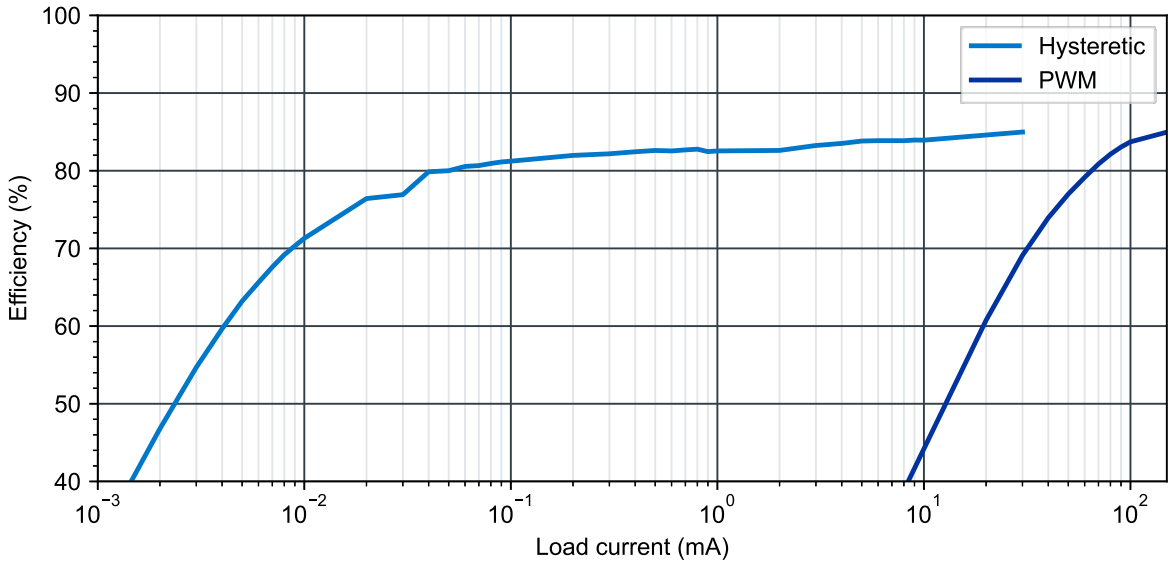


Figure 8: BUCK1 efficiency vs. load current (VIN_{BUCK1} = 3.8 V, VO1 = 0.8 V)

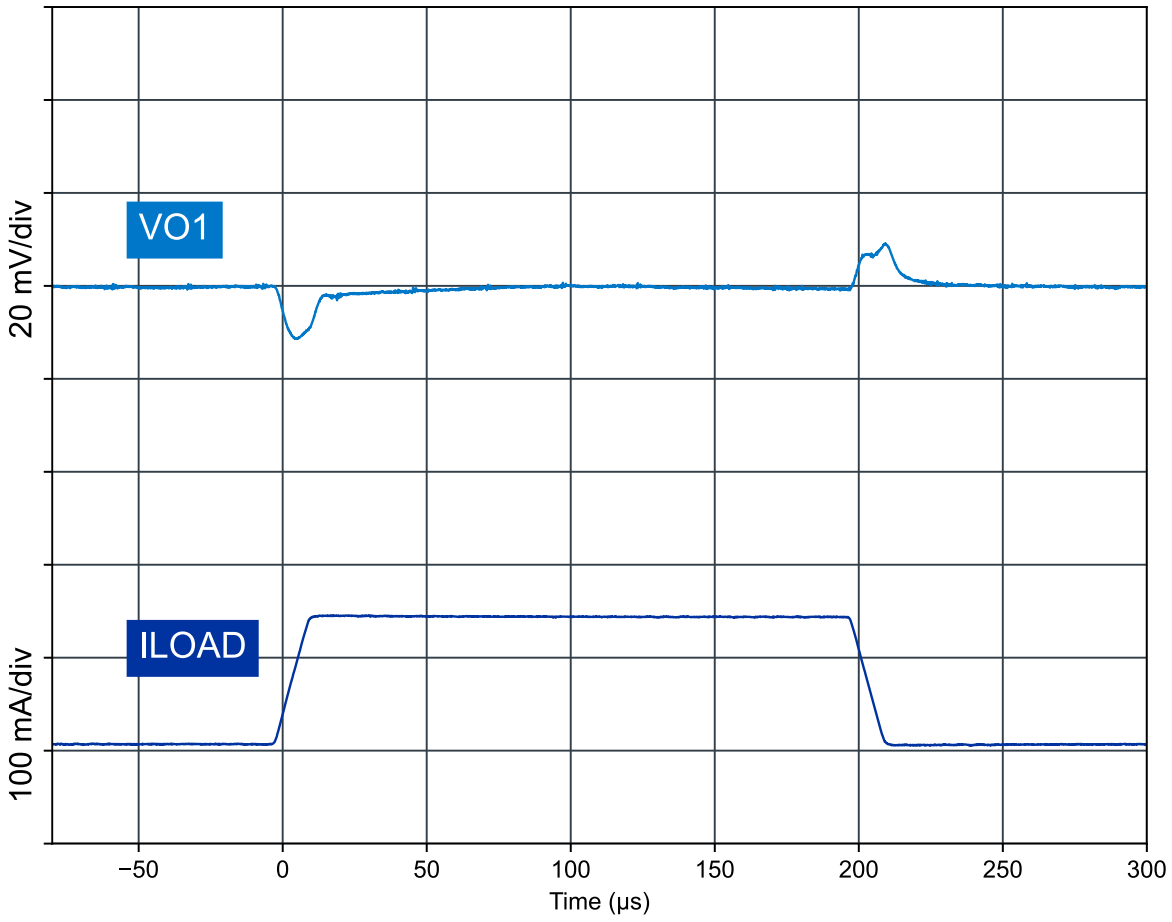


Figure 9: BUCK1 load transient (VIN_{BUCK1} = 3.8 V, VO1 = 0.8 V, I_{LOAD} 10 mA - 150 mA)

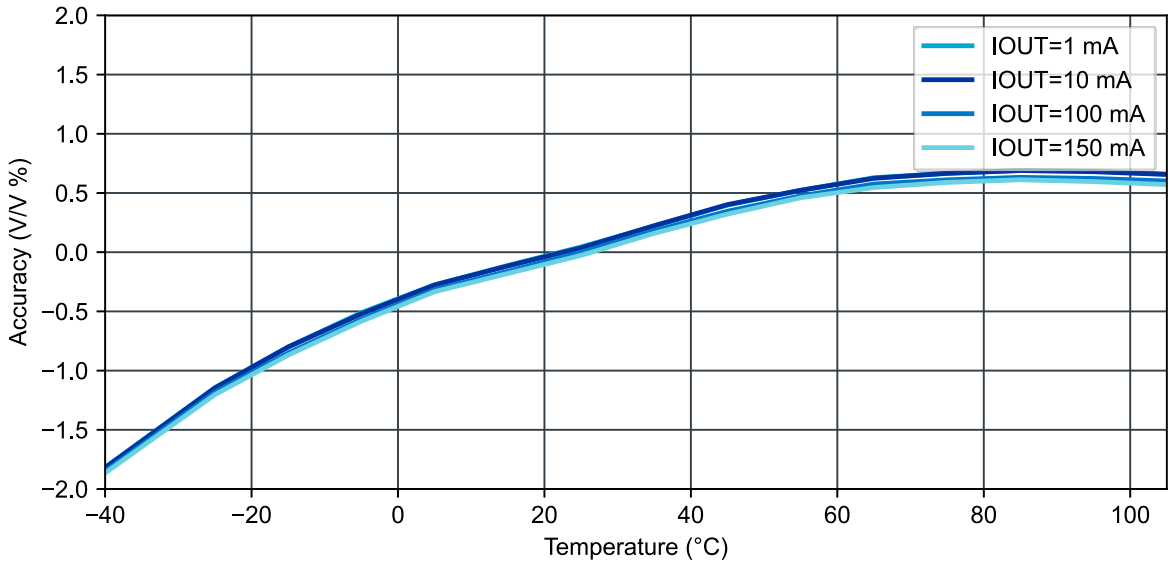


Figure 10: VO1 vs. temperature (VIN_{BUCK1} = 3.8 V, VO1 = 0.8 V)

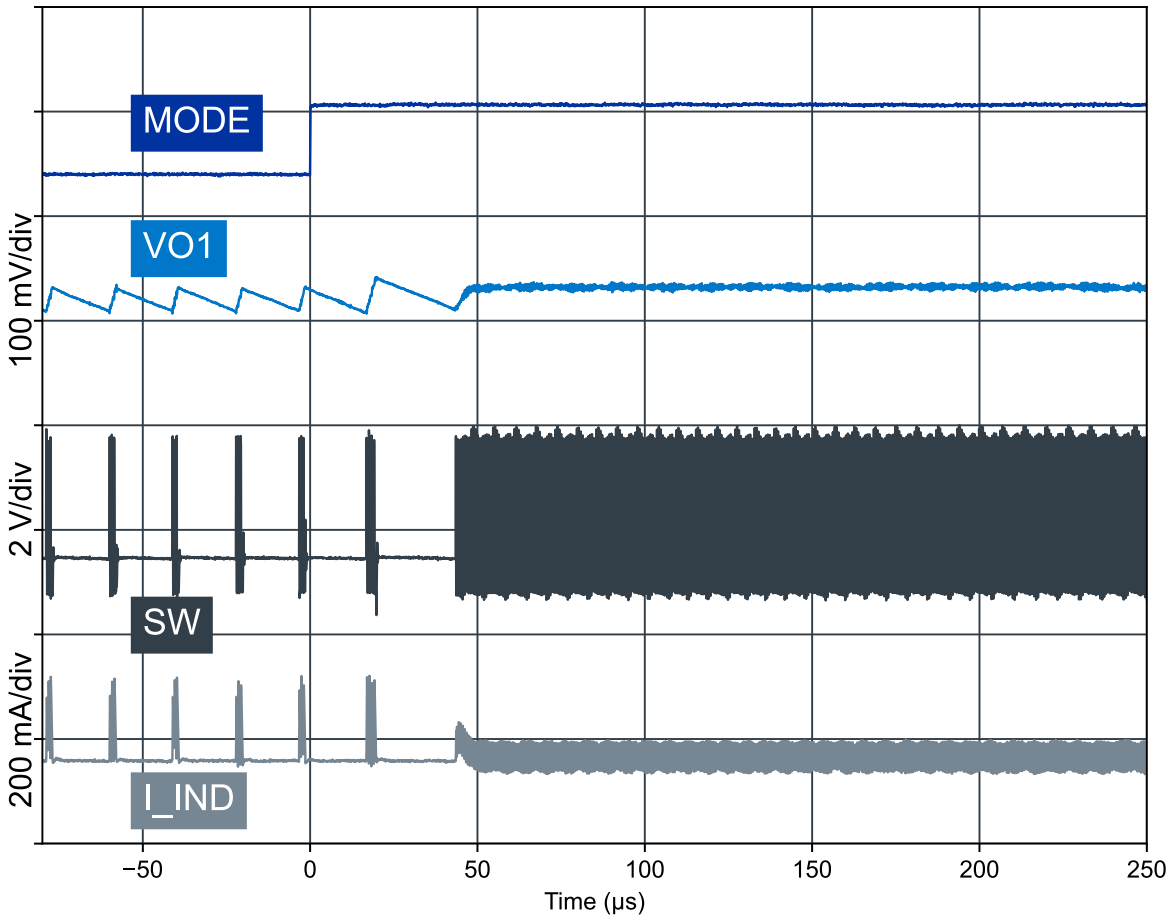


Figure 11: Mode transition from hysteretic to PWM (VIN_{BUCK1} = 3.8 V, VO1 = 0.8 V, I_OUT = 10 mA)

6.1.3 BUCK2

BUCK2 is an always-on buck regulator. It is running when VIN is above the Power-on reset threshold, **ENABLE** is HIGH, and the external components are present.

The default output voltage for BUCK2 is 1.2 V. The regulator can supply load currents up to 150 mA in PWM mode and up to 30 mA in Hysteretic mode. The output voltage can be programmed in 50 mV steps between 1.2 V and 1.4 V. Output voltage settings for both PWM and Hysteretic mode must be identical.

The following registers are for BUCK2 output voltage programming:

Register	Description
BUCK2.VOUT.ULP	Output voltage setting in hysteretic mode
BUCK2.VOUT.PWM	Output voltage setting in PWM mode
TASKS_UPDATE_VOUTPWM	Task for applying a new BUCK2VOUTPWM register value.

Table 13: BUCK2 output voltage registers

The (decimal) code for a given output voltage VO2 can be calculated using equation Code = 10 + (VO2 - 1.2 V) / 0.05 V.

To change output voltage while BUCK2 is running, BUCK2 must be set first to PWM mode before writing a new setting. This ensures a smooth voltage ramp. Hysteretic mode can be used again after a trigger task.

6.1.3.1 Electrical specification

Symbol	Description	Min.	Typ.	Max.	Units
VIN_{BUCK2}	Regulator input voltage	3.0		5.5	V
VO2	Regulator output voltage range	1.2		1.4	V
$VO2_{STEP}$	Output voltage programming step		50		mV
$VACC_{PWM}$	Output voltage accuracy Average voltage, not including ripple or transients PWM mode	-5		5	%
$VACC_{H}$	Output voltage accuracy Average voltage, not including ripple or transients Hysteretic mode	-5		-5	%
I_{OUT_PWM}	Output current range, PWM mode	0		150	mA
I_{OUT_H}	Output current range, Hysteretic mode	0		30	mA
VO_{RIPPLE_H}	Output voltage peak-to-peak ripple in Hysteretic mode		50		mV
VO_{RIPPLE_PWM}	Output voltage peak-to-peak ripple in PWM mode			10	mV
$LOAD_{TR}$	Load transient regulation I_{OUT} rises or falls between 10 mA - 150 mA in 10 µs PWM mode	-50		50	mV
$LINE_{TR}$	Line transient regulation VIN_{BUCK2} voltage rises or falls 300 mV in 10 µs with 1 kHz rate PWM mode		+/- 10		mV
EFF_{100MA}	BUCK efficiency with 100 mA load current VIN_{BUCK2} = 3.8 V, VO2 = 1.2 V, T = 25°C PWM mode		87		%

Table 14: BUCK2 electrical specification

6.1.3.2 Electrical characteristics

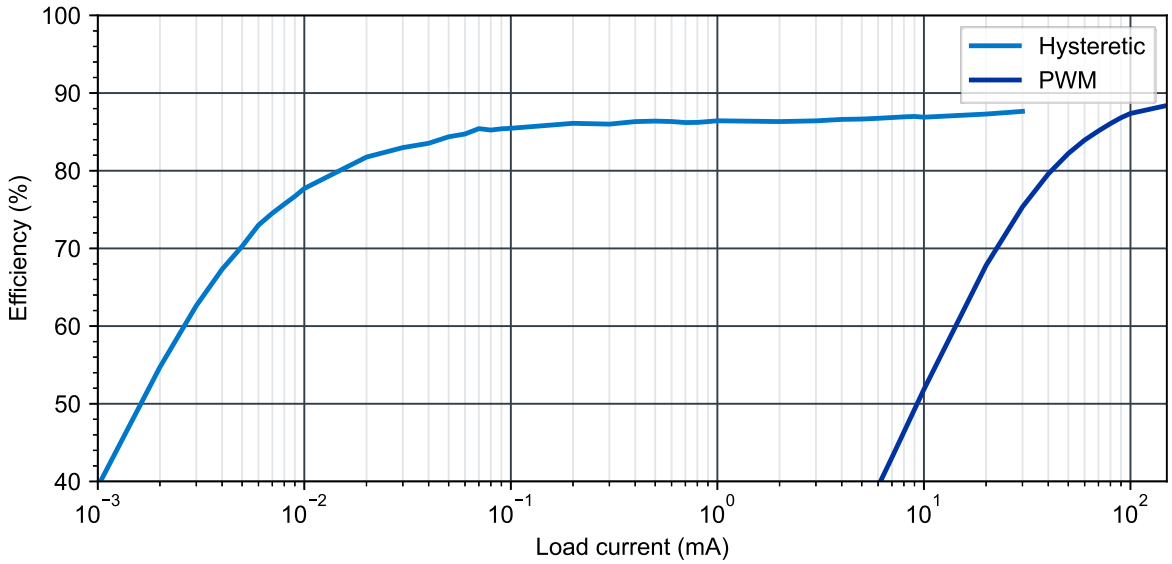


Figure 12: BUCK2 efficiency vs. load current (VIN_{BUCK2} = 3.8 V, VO2 = 1.2 V)

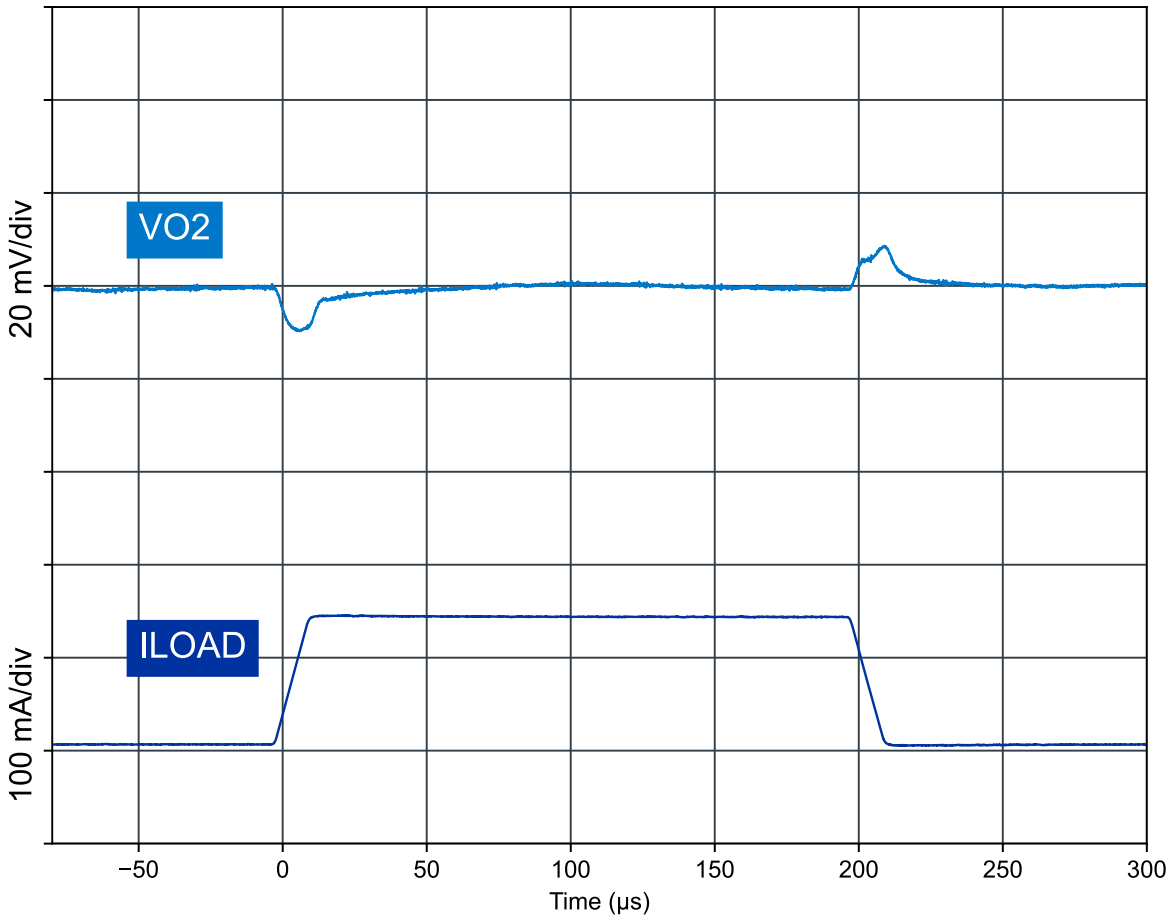


Figure 13: BUCK2 load transient (VIN_{BUCK2} = 3.8 V, VO2 = 1.2 V, I_{LOAD} 10 mA - 150 mA)

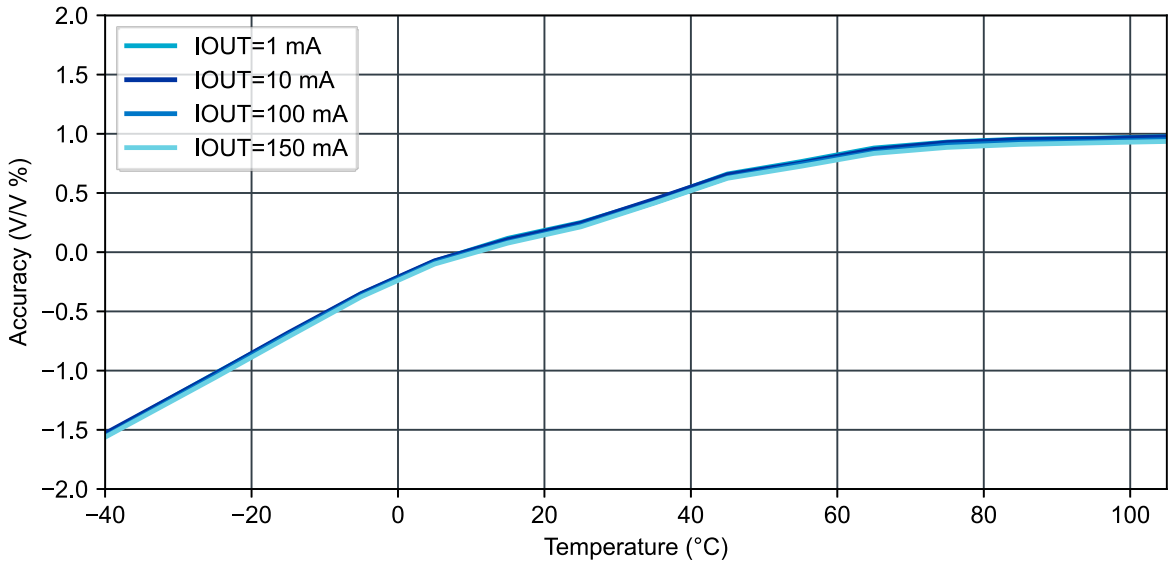


Figure 14: VO2 vs. temperature (VIN_{BUCK2} = 3.8 V, VO2 = 1.2 V)

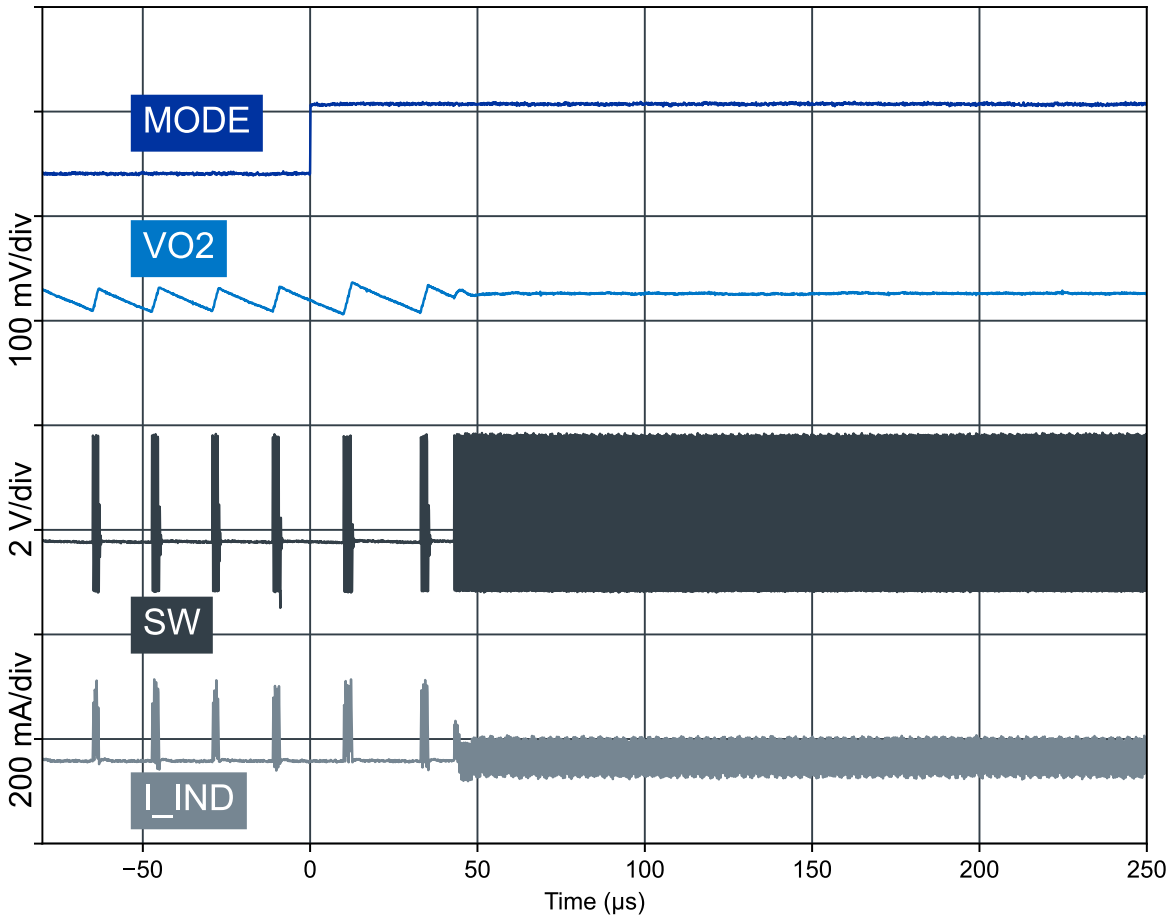


Figure 15: Mode transition from hysteretic to PWM (VIN_{BUCK2} = 3.8 V, VO2 = 1.2 V, I_OUT = 10 mA)

6.1.4 BUCK3

BUCK3 is not enabled by default.

BUCK3 is controlled through the TWI and is by default set to Hysteretic mode. It can supply up to 550 mA in PWM mode and up to 10 mA in Hysteretic mode. The output voltage is controlled by a DAC and can be programmed in 25 mV steps between 0.5 V and 3.3 V.

BUCK3 must start up in Hysteretic mode, meaning that the load must not exceed 10 mA during startup. It is strongly recommended to set BUCK3 to PWM once it has started.

The following registers control BUCK3:

Register	Description
BUCK3.VOUT	Output voltage setting (for both modes)
BUCK3.SEL.DAC	Enabling the DAC
TASKS_START_BUCK3	Enabling the BUCK
BUCK3.CONF.PWM.MODE	Entering PWM mode
TASKS_STOP_BUCK3	Disabling the BUCK

Table 15: BUCK3 control registers

The (decimal) code for a given output voltage VO3 can be calculated using equation Code = (VO3 - 0.5 V) / 0.025 V.

Note: Dynamic voltage adjustment while BUCK3 is operating is not recommended.

6.1.4.1 Electrical specification

Symbol	Description	Min.	Typ.	Max.	Units
VIN_{BUCK3}	Regulator input voltage	3.0		5.5	V
VO3	Regulator output voltage range	0.5		3.3	V
$VO3_{STEP}$	Output voltage programming step		25		mV
VDO3	Drop out voltage (I_{OUT} = 500 mA)		150		mV
VACC	Output voltage accuracy Average voltage, not including ripple or transients PWM mode	-6		2	%
I_{OUT_PWM}	Output current range, PWM mode	0		550	mA
I_{OUT_H}	Output current range, Hysteretic mode	0		10	mA
$VO3_{RIPPLE\_H}$	Output voltage peak-to-peak ripple in Hysteretic mode		50		mV
$VO3_{RIPPLE\_PWM}$	Output voltage peak-to-peak ripple in PWM mode over output current range and VIN_{BUCK} - VO3 > 1.0 V			25	mV
$LOAD_{TR}$	Load current transient Load current T_{rise}=T_{fall}=1 µs, VO3=1.3 V, I_{load} 30 mA - 150 mA PWM mode	-50		50	mV
$LINE_{TR}$	Line transient regulation VIN_{BUCK3} voltage rises or falls 300 mV in 10 µs with 1 kHz rate PWM mode		+/-15		mV
EFF_{200MA}	BUCK3 efficiency with 200 mA load current VIN_{BUCK3} = 3.8 V, VO3 = 3.3 V, T = 25°C PWM mode		93		%
t_{START}	Startup time (VO3 = 3.3 V)			200	µs

Table 16: BUCK3 electrical specification

6.1.4.2 Electrical characteristics

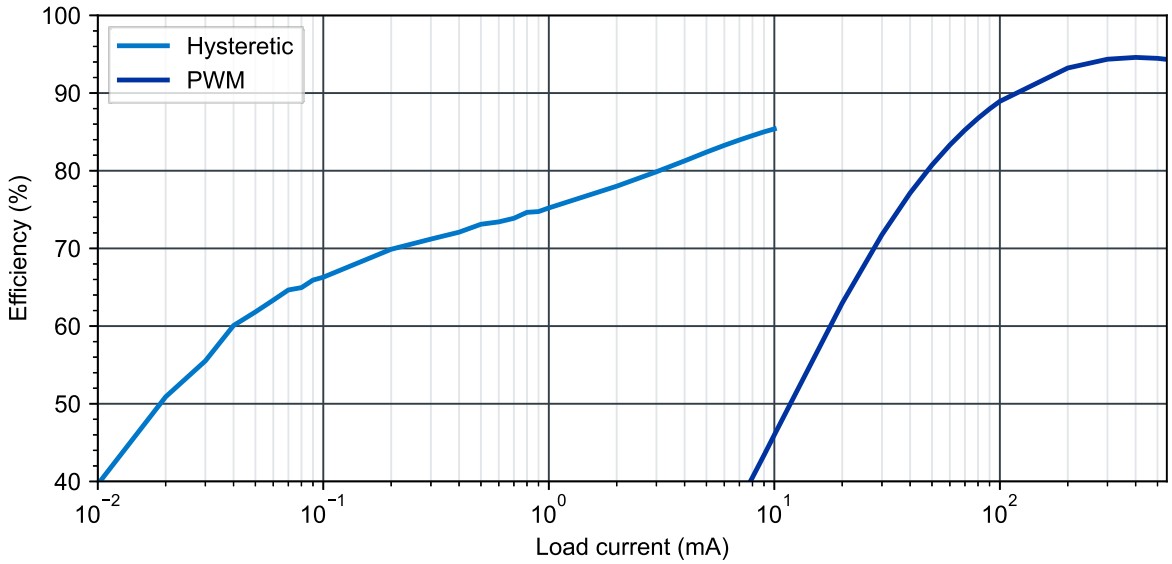


Figure 16: BUCK3 efficiency vs. load current (VIN_{BUCK3} = 3.8 V, VO3 = 3.3 V)

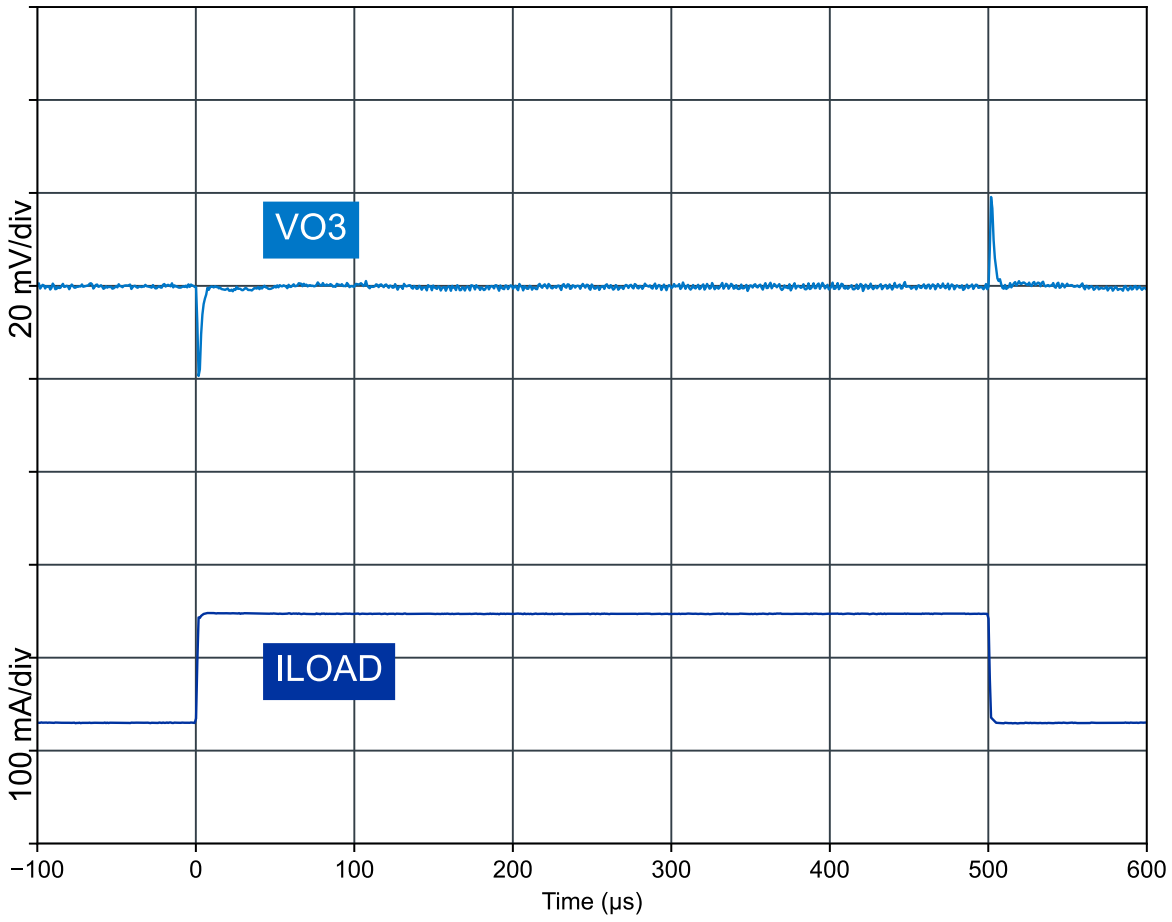


Figure 17: BUCK3 load transient (VIN_{BUCK3} = 3.8 V, VO3 = 1.3 V, I_{load} 30 mA - 150 mA)

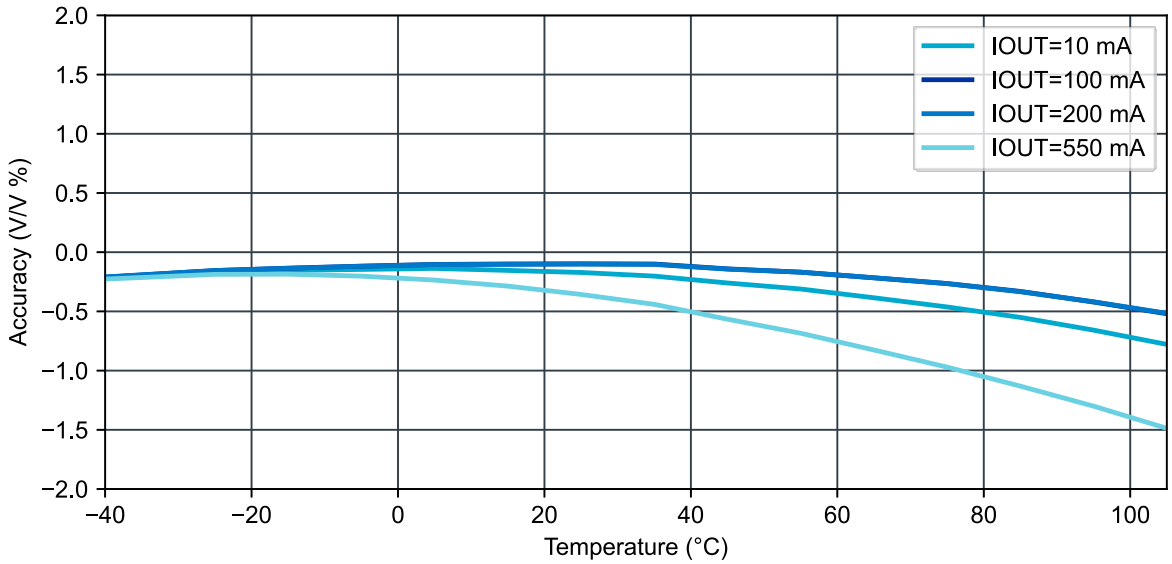


Figure 18: V03 vs. temperature (VIN_{BUCK3} = 3.8 V, VO3 = 3.3 V)

6.2 LDO0

LDO0 is a general purpose linear low dropout regulator. It is fully controlled by the host system through TWI.

LDO0 output voltage is set in register LDO0.VOUT and can be 1.8 V up to 3.3 V in 300 mV steps. The default voltage is 3 V. It supports a load current of up to 30 mA and is set in register TASKS_START_LDO0.

6.2.1 Electrical specification

Symbol	Description	Min.	Typ.	Max.	Units
VIN_{LDO0}	Regulator input voltage	3.0		5.5	V
VLDO0	Regulator output voltage		1.8, 2.1, 2.41, 2.7, 3.0, 3.3		V
$VACC_{LDO0}$	Output voltage accuracy	-3		3	%
VDO	Dropout voltage I_{OUT} = 30 mA		200		mV
I_{OUT}	Load current output range	0		30	mA
$LOAD_{TR}$	Load transient regulation I_{OUT} rises or falls between 0 mA - 30 mA in 10 µs		+/-25		mV
$LINE_{TR}$	Line transient regulation VIN_{LDO0} voltage rises or falls 300 mV in 10 µs with 1 kHz rate		+/-10		mV
I_Q	Quiescent current, no load At least one BUCK[0..2] running in PWM mode		80		µA
t_{START}	Startup time (VLDO0 = 3.3 V)			500	µs

Table 17: LDO0 electrical specification

6.2.2 Electrical characteristics

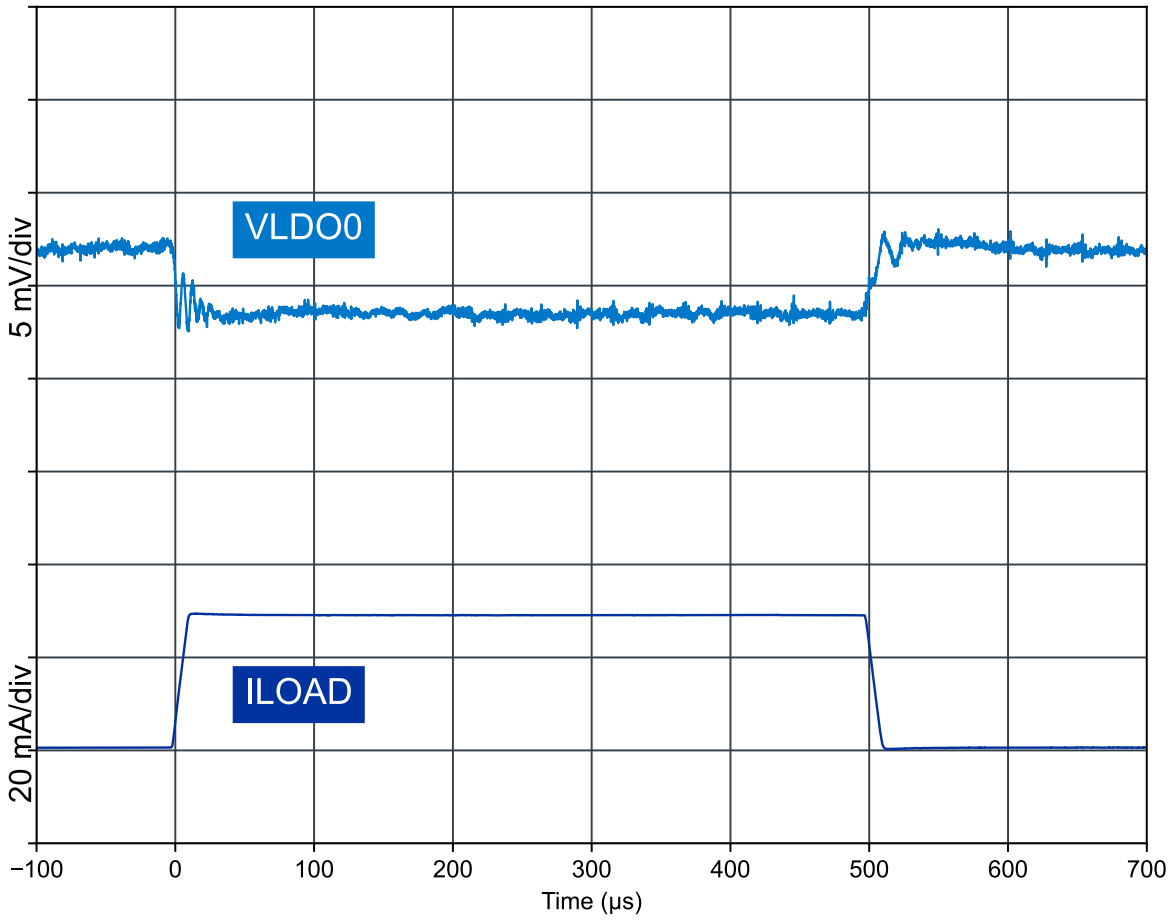


Figure 19: LDO0 load transient (VLDO0 = 3.0 V, I_{load} 0 mA - 30 mA)

6.3 LDO1

LDO1 is a general purpose linear low dropout regulator. It is fully controlled by the host system through TWI.

LDO1 delivers 1.8 V output voltage with very low quiescent power consumption. It supports up to 15 mA load currents that can be set in register TASKS_START_LDO1.

6.3.1 Electrical specification

Symbol	Description	Min.	Typ.	Max.	Units
VIN_{LDO1}	Regulator input voltage	3.0		5.5	V
VLDO1	Regulator output voltage	1.62	1.8	1.98	V
I_{OUT}	Average load current output range	0		15	mA
$LOAD_{TR}$	Load transient regulation I_{OUT} rises or falls between 0 mA - 15 mA in 10 µs		+/-10		mV
$LINE_{TR}$	Line transient regulation VIN_{LDO1} voltage rises or falls 300 mV in 10 µs with 1 kHz rate		+/-10		mV
I_Q	Quiescent current, no load All active BUCKs (BUCK[0..2]) running in Hysteretic mode		1.6		µA
	Quiescent current, no load At least one BUCK[0..2] running in PWM mode		22		µA
t_{START}	Startup time			300	µs

Table 18: LDO1 electrical specification

6.3.2 Electrical characteristics

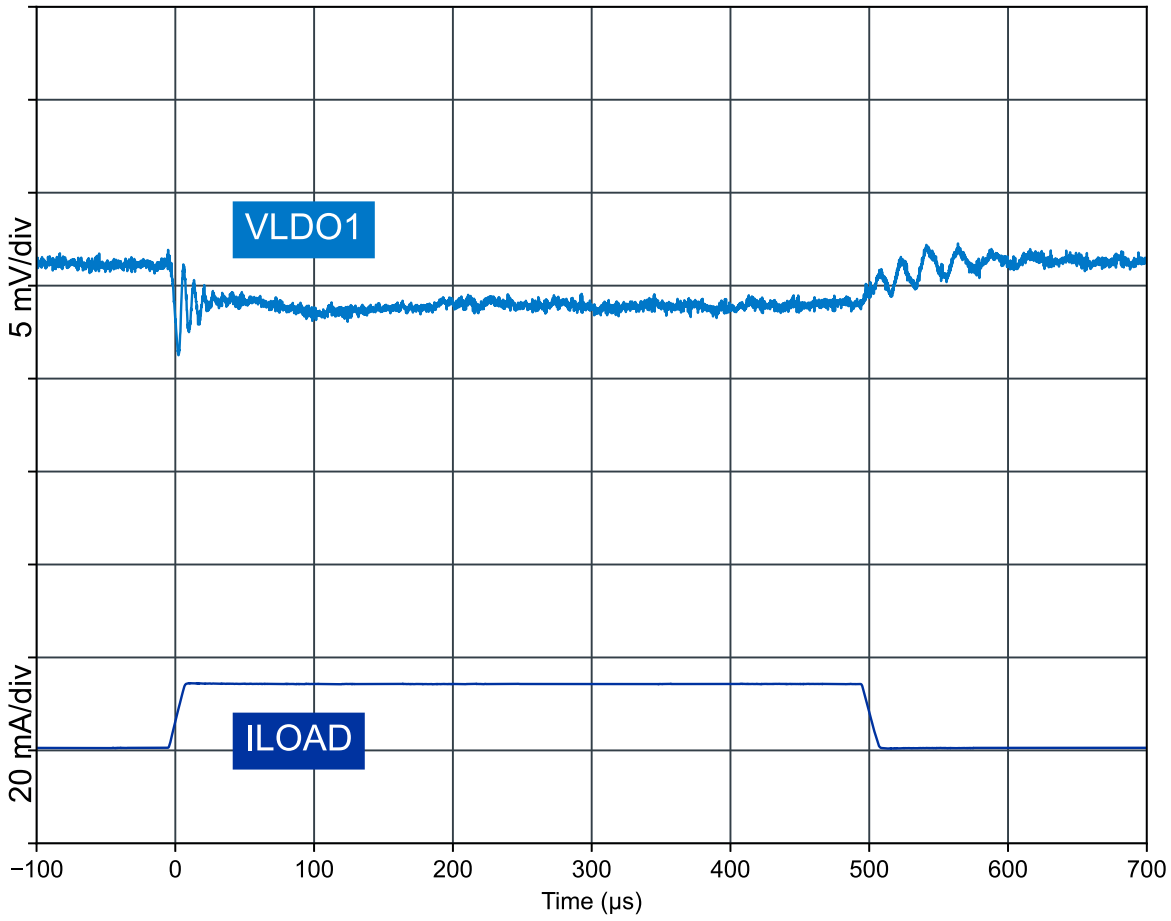


Figure 20: LDO1 load transient (VLDO1 = 1.8 V, I_{load} 0 mA - 15 mA)

6.4 Power-on reset

When VIN rises above VIN_{VTH1_RISE}, a power-on reset (POR) occurs. The chip starts up when the **ENABLE** pin is HIGH.

When VIN falls below VIN_{VTH1_FALL}, the chip shuts down.

6.4.1 Electrical specification

Symbol	Description	Min.	Typ.	Max.	Units
VIN_{VTH1_RISE}	Threshold voltage for rising supply	2.8	2.9	3.0	V
VIN_{VTH1_FALL}	Threshold voltage for falling supply	2.7	2.8	2.9	V

Table 19: Power-on reset electrical specification

7 SYSTEM — System components

SYSTEM features complement the power supply. Thermal protection can be enabled and set to provide a warning interrupt when the die temperature is too high. In the case of extreme temperature, the chip shuts down to prevent damage.

A watchdog timer can be set to provide a reset to the host if firmware is unresponsive.

Hibernate mode is the lowest power operating mode of the chip. It reduces the quiescent current of the device to extend battery life. The device will automatically wake-up after a pre-configured timeout.

Three general purpose I/Os are available and can be configured to control off-chip sensors or power supplies.

7.1 Thermal protection

Thermal protection prevents permanent damage to the chip and provides a warning to the host system when the chip overheats. It is enabled and configured through TWI.

Thermal protection monitors the on-chip temperature sensor element. When in an active power mode with an expected high current load, thermal protection must be enabled through registers to save power. An example is when BUCK is running in PWM mode. Register TH.DYN.POWERUP configures the thermal sensor and selects which BUCK will activate the thermal sensor during PWM mode.

During startup, thermal protection is always enabled with T_{LOW_RISE} and T_{LOW_FALL} thresholds. If the temperature is higher than T_{LOW_RISE}, startup is halted until the temperature falls below T_{LOW_FALL}.

When startup is complete and the **READY** pin is set, the temperature thresholds are changed to T_{HIGH_RISE} and T_{HIGH_FALL}. Thermal warning and thermal shutdown are disabled by default after startup.

Thermal warning must be enabled in register INTENSET0 for the device to send an interrupt to the host system when the chip temperature rises over T_{HIGH_RISE}.

Thermal shutdown must be enabled separately for the device to shutdown when the temperature rises above $T_{SHUTDOWN}$. The device starts up again once the die cools down.

7.1.1 Electrical specification

Symbol	Description	Min.	Typ.	Max.	Units
$T_{SHUTDOWN}$	Shutdown threshold temperature		140		C
T_{HIGH_RISE}	Rising temperature threshold in normal operation		115		C
T_{HIGH_FALL}	Falling temperature threshold in normal operation		107		C
T_{LOW_RISE}	Rising temperature threshold in startup		107		C
T_{LOW_FALL}	Falling temperature threshold in startup		102		C

Table 20: Thermal protection electrical specification

7.2 Watchdog

The watchdog timer generates a reset when the system is stalled and no internal watchdog is running during sleep.

By default, the watchdog is disabled after startup. The watchdog is configured and enabled through TWI. Once enabled, the watchdog uses the 2 kHz clock as a counter. The value for the watchdog trigger target can be programmed from 4 seconds up to 776.7 days in 4 second intervals. The watchdog and wakeup timer share the same counter, but only one timer can be active at a time.

When the watchdog is configured and enabled, the host periodically resets the counter before it reaches the trigger value. If the host is not able to reset the counter, the watchdog will reach the trigger value. The device will pull down the **READY** pin and reset, including the watchdog. After this reset and power cycle, the device then starts up again.

WDTRIGGERVALUE[23:0]	Programmed time
24'h000000	Initialization value (do not use)
24'h000001	0 s (do not use)
24'h000002	4 s
24'h000003	8 s
...	...
24'hFFFFFD	~776.7 d – 4 s
24'hFFFFFE	~776.7 d
24'hFFFFFF	~776.7 d + 4 s

Table 21: Trigger values for the watchdog and wakeup timers

Note: The programmed target time may vary ±40% due to process and temperature variations.

7.3 Hibernate mode

Hibernate mode is configured, started, and controlled through the TWI. It is the lowest power mode and uses only 200 nA.

The device enters Hibernate mode by configuring the watchdog and writing to register WD.REQ.POWERDOWN. All BUCKs are turned off and the device enters a low power state. The TWI is not accessible from software during Hibernate mode.

The oscillator and timer circuits are the only components active in this mode. The **ENABLE** pin must be connected to VIN. The watchdog timer must be configured as a wake up source before entering this mode. The device powers up after the timer expires.

The wakeup timer can be programmed from 4 seconds up to 776.7 days in 4 second intervals, see Trigger values for the watchdog and wakeup timers on page 37.

When the wakeup timer reaches its target value, the device powers up.

7.4 Pin controls

ENABLE input pin

The chip starts up when **ENABLE** is pulled to VIN. Pulling down **ENABLE** shuts down the device, resets all registers and reduces power consumption from VIN supply. See Electrical specification CMOS mode on page 39 for more information.

READY pin

The **READY** pin is an open-drain pin. Logic HIGH on **READY** means that the device has started up (all BUCK regulators are on) and is ready for use. Ready goes LOW when the device shuts down. See Electrical specification CMOS mode on page 39 for more information.

TWI serial interface pins

Device control is managed through an I2C compatible TWI serial interface and registers on the chip. The device has a serial data I/O signal SDA and a clock input signal SCL. The **VDD_TWI** pin supplies 1.8 V to the TWI. The startup sequence activates TWI when **READY** is HIGH. TWI configures **SDA** pin output drive strength through register PADDRIVESTRENGTH[5].

TWI configures and controls the thermal sensor, regulators, watchdog, and wakeup timer functions. The values found in Electrical specification Schmitt trigger mode on page 41 apply to SDA and SCL pins. The pins are referenced to VDD_{TWI} level.

Interrupt pin

nINT is an active LOW, open drain interrupt pin. The TWI interface configures, reads, and clears nINT.

BUCK_MODE input pins

BUCK_MODE[n] pins toggle the power mode for BUCK[n]. Register SWREADY on page 58 must be written to enable the pins. **BUCK_MODE[n]** pins are configured as Schmitt trigger inputs by default, see Electrical specification Schmitt trigger mode on page 41. CMOS input is also available, see Electrical specification CMOS mode on page 39.

BUCK0 is forced to PWM mode by default when $BUCK_{MODE0}$ or $BUCK_{MODE1}$ input is HIGH and SWREADY=1. BUCK1 and BUCK2 use the $BUCK_{MODE1}$ input pin state. BUCK3 uses the $BUCK_{MODE2}$ input pin state.

BUCK_MODE[n] pins use VO2 when configured to Schmitt trigger mode. When in CMOS mode, VIN is used as reference. See Electrical specification CMOS mode on page 39 for more information.

GPIO - general purpose input/output

GPIO[n] are general purpose input/output pins that are available to the host. After startup, the **GPIO[n]** pins are disabled and set to high-impedance mode by default. The dedicated pin supply, **VIN_GPIO**, must be connected to **VIN**.

The pins are set to VIN_{GPIO} when used in CMOS mode, see Electrical specification CMOS mode on page 39. In Schmitt trigger mode, the pins are set to VO2. See Electrical specification Schmitt trigger mode on page 41 for more information about **GPIO[n]** pins.

7.5 I/O Drivers

This chapter describes the electrical specifications for I/Os.

7.5.1 Electrical specification CMOS mode

This section is valid for **ENABLE**, **READY**, **nINT**, **SCL**, **SDA**, **GPIO[n]**, and **BUCK_MODE[n]** pins when put in CMOS mode.

Symbol	Description	Min.	Typ.	Max.	Units
V_{IO}	I/O driver power supply (**VIN**, **VIN_GPIO**) I/O driver power supply for the TWI (**VDD_TWI**) I/O driver supply for open-drain pins **READY** and **nINT** (**VOO_IN**)	3.0 1.62 1.62		5.5 1.95 3.47	V
V_{IL}	Input low voltage			$0.18V_{IO}$	V
V_{IH}	Input high voltage	$0.89V_{IO}$			V
V_{OL}	Output low voltage			$0.55V_{IO}$	V
V_{OH}	Output high voltage	$0.62V_{IO}$			V
$I_{OL,5V,LS}$	Output current, normal strength, VIO=5 V		4.4		mA
$I_{OL,5V,HS}$	IOL output current, high strength, VIO=5 V		18		mA
$I_{OH,5V,LS}$	IOH output current, normal strength, VIO=5 V		8		mA
$I_{OH,5V,HS}$	IOH output current, high strength, VIO=5 V		29		mA
$R_{PU,5V}$	I/O pull-up resistor, when enabled VIO=5 V	50	77	132	kΩ
$R_{PD,5V}$	I/O pull-down resistor, when enabled VIO=5 V	58	99	213	kΩ
$I_{OL,3V3,LS}$	Output current, normal strength, VIO=3.3 V		3		mA
$I_{OL,3V3,HS}$	Output current, high strength, VIO=3.3 V		13		mA
$I_{OH,3V3,LS}$	Output current, normal strength, VIO=3.3 V		4.5		mA
$I_{OH,3V3,HS}$	Output current,high strength, VIO=3.3 V		17		mA
$R_{PU,3V3}$	I/O pull-up resistor, when enabled, VIO=3.3 V	76	124	219	kΩ
$R_{PD,3V3}$	I/O pull-down resistor, when enabled VIO=3.3 V	92	173	382	kΩ
$I_{OL,2V5,LS}$	Output current, normal strength, VIO=2.5 V		3.2		mA
$I_{OL,2V5,HS}$	Output current, high strength, VIO=2.5 V		13		mA
$I_{OH,2V5,LS}$	Output current, normal strength, VIO=2.5 V		2.7		mA
$I_{OH,2V5,HS}$	Output current, high strength, VIO=2.5 V		10		mA
$R_{PU,2V5}$	I/O pull-up resistor, when enabled VIO=2.5 V	150	181	333	kΩ

Symbol	Description	Min.	Typ.	Max.	Units
$R_{PD,2V5}$	I/O pull-down resistor, when enabled VIO=2.5 V	139	278	626	kΩ
$I_{OL,1V8,LS}$	Output current, normal strength, VIO=1.8 V		1.4		mA
$I_{OL,1V8,HS}$	Output current, high strength, VIO=1.8 V		5.5		mA
$I_{OH,1V8,LS}$	Output current, normal strength, VIO=1.8 V		1.1		mA
$I_{OH,1V8,HS}$	Output current, high strength, VIO=1.8 V		4		mA
$R_{PU,1V8}$	I/O pull-up resistor, when enabled VIO=1.8 V	173	321	604	kΩ
$R_{PD,1V8}$	I/O pull-down resistor, when enabled VIO=1.8 V	266	570	1277	kΩ

Table 22: CMOS mode electrical specification

7.5.2 Electrical specification Schmitt trigger mode

This section is valid for **`BUCK_MODE[n]`** and **`GPIO[n]`** pins when they are configured as Schmitt trigger inputs.

Symbol	Description	Min.	Typ.	Max.	Units
VT_{POS}	Positive going input voltage threshold (**VO2**=1.2 V)	0.7		0.9	V
VT_{NEG}	Negative going input voltage threshold (**VO2**=1.2 V)	0.35		0.65	V
D_{VT}	Hysteresis (VT_{POS} - VT_{NEG}) (**VO2**=1.2 V)		0.3		V

Table 23: Schmitt trigger mode electrical specification

8 Hardware and layout

8.1 Pin assignments

The ball assignment figure and table describe the assignments for the chip.

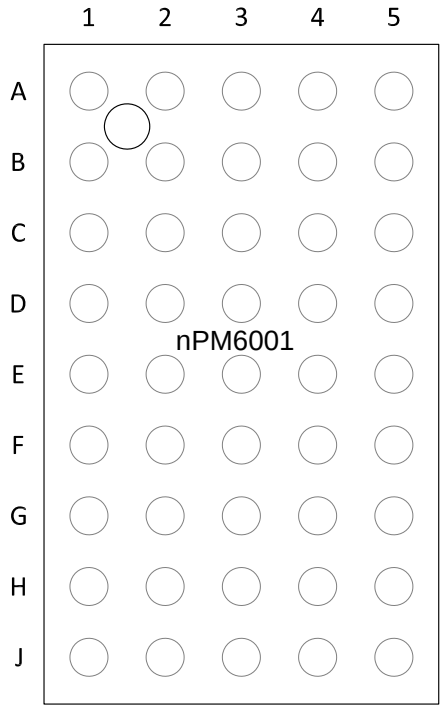


Figure 21: WLCSP ball assignments, top view

Pin	Name	Function	Description
A1	VIN_BUCK2	Power	Input supply for BUCK2
A2	SW2	Power	BUCK2 regulator output (to inductor)
A3	AVSS1_2	Power	Ground (BUCK1 and BUCK2)
A4	SW1	Power	BUCK1 regulator output (to inductor)
A5	VIN_BUCK1	Power	Input supply for BUCK1
B1	VO2	Power	BUCK2 regulator output
B2	ENABLE	Digital IN	Enable input
B3	RESERVED	Reserved	Connect to ground
B4	RESERVED	Reserved	Do not connect
B5	VO1	Power	BUCK1 regulator output
C1	VIN_LDO0	Power	Input supply for LDO0
C2	GPIO0	Digital I/O	General purpose input/output pin
C3	RESERVED	Reserved	Connect to VO0
C4	VDD_TWI	Power	Input supply for TWI
C5	VLDO1	Power	LDO1 regulator output
D1	VLDO0	Power	LDO0 regulator output
D2	GPIO2	Digital I/O	General purpose input/output pin
D3	GPIO1	Digital I/O	General purpose input/output pin
D4	nINT	Digital OUT	Open-drain Interrupt output, active low
D5	VIN_LDO1	Power	Input supply for LDO1
E1	VIN_GPIO	Power	Input supply for general purpose pins
E2	SDA	Digital I/O	TWI data input/output
E3	SCL	Digital IN	TWI clock input
E4	RESERVED	Reserved	Do not connect
E5	RESERVED	Reserved	Connect to ground
F1	AVSS	Power	Ground
F2	AVSS_ANA	Power	Ground
F3	VIN_ANA	Power	Input supply
F4	RESERVED	Reserved	Connect to ground
F5	BUCK_MODE1	Digital IN	BUCK operating mode control input
G1	VIN	Power	Input supply
G2	BUCK_MODE0	Digital IN	BUCK operating mode control input
G3	RESERVED	Reserved	Connect to ground
G4	BUCK_MODE2	Digital IN	BUCK operating mode control input

Pin	Name	Function	Description
G5	VO0_IN	Power	Input supply for the control inputs and outputs
H1	VO3	Power	BUCK3 regulator output
H2	RESERVED	Reserved	Connect to ground
H3	AVSS0	Power	Ground (BUCK0)
H4	READY	Digital OUT	Open-drain Ready output, active high
H5	VO0	Power	BUCK0 regulator output
J1	VIN_BUCK3	Power	Input supply for BUCK3
J2	SW3	Power	BUCK3 regulator output (to inductor)
J3	AVSS3	Power	Ground (BUCK3)
J4	SW0	Power	BUCK0 regulator output (to inductor)
J5	VIN_BUCK0	Power	Input supply for BUCK0

Table 24: Pin assignments

8.2 Mechanical specifications

The mechanical specifications for the package shows the dimensions in millimeters.

8.2.1 WLCSP 2.175x3.635 mm package

Dimensions in millimeters for the WLCSP 2.175x3.635 mm package. The package includes backside coating (BSC).

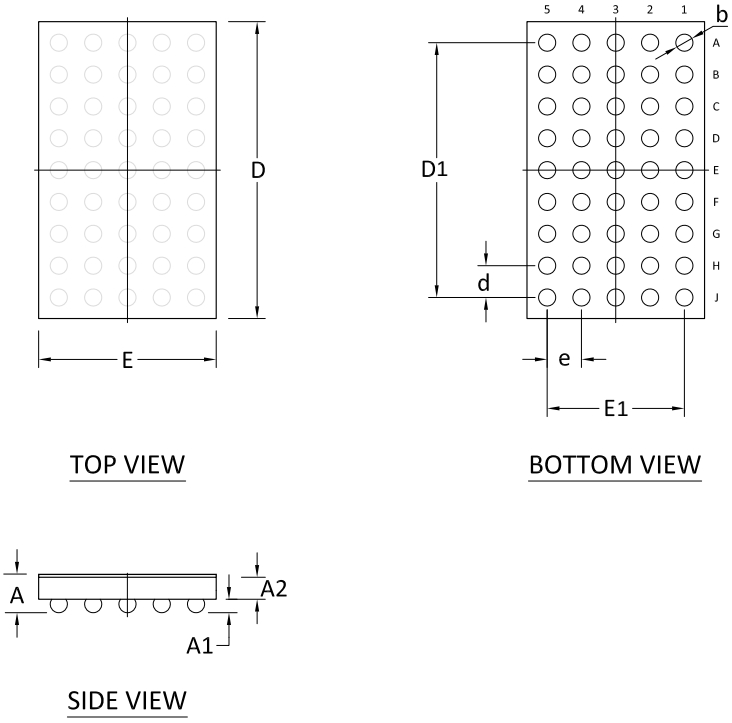


Figure 22: WLCSP 2.175x3.635 mm package

	A	A1	A2	D	E	D1	E1	b	d	e
Min.	0.376	0.135	0.219	-	-	-	-	-	-	-
Nom.	0.434	-	0.244	3.635	2.175	3.12	1.68	0.21	0.39	0.42
Max.	0.492	0.195	0.269	-	-	-	-	-	-	-

Table 25: WLCSP dimensions in millimeters

8.3 Reference circuitry

Documentation for the different package reference circuits, including Altium Designer files, PCB layout files, and PCB production files can be downloaded from www.nordicsemi.com.

The following reference circuits for nPM6001 show the schematics and components to support different configurations in a design.

	Configuration 1	Configuration 2	Configuration 3
Description	Default configuration All power regulators in use	Normal configuration Only BUCK1 and LDO0 in use	Minimal configuration Only BUCK0 in use
BUCK0	Configured	Configured	Configured
BUCK1	Configured	Configured	Not used Connect **VO1** to VIN
BUCK2	Configured	Not used Connect **VO2** to **VO0**	Not used Connect **VO2** to **VO0**
BUCK3	Configured	Not used	Not used
LDO0	Configured	Configured	Not used
LDO1	Configured	Not used	Not used

Table 26: PCB application configuration

8.3.1 Configuration 1

The reference schematic and bill of materials for the default configuration are shown here.

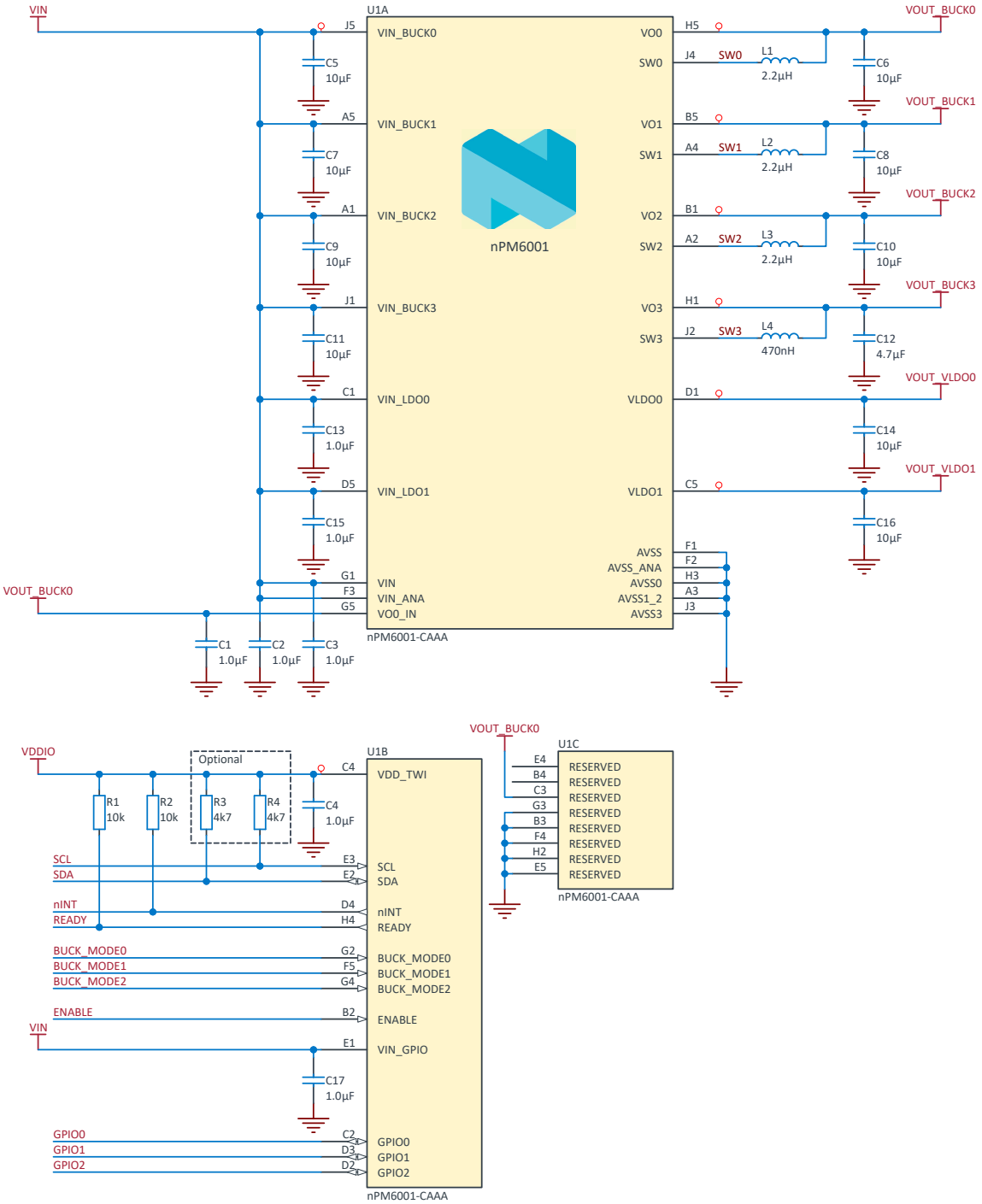


Figure 23: Reference application schematics, configuration 1

In this configuration, the **ENABLE** pin is connected to VIN. When the input voltage rises above VIN_{VTH1_RISE}, the buck regulators start up in the following order:

- BUCK0 with 1.8 V output voltage
- BUCK1 with 0.8 V output voltage
- BUCK2 with 1.2 V output voltage

BUCK[0..2] regulators start in PWM mode to ensure that the application system has enough power to start up. Once buck regulators are running, the **READY** pin is set.

The device can also be started with the **ENABLE** input pin. In this configuration, the **ENABLE** pin is disconnected from VIN and controlled by a circuitry that pulls **ENABLE** to VIN or ground level. Rising edge of the **ENABLE** triggers startup sequence if VIN is within specified range.

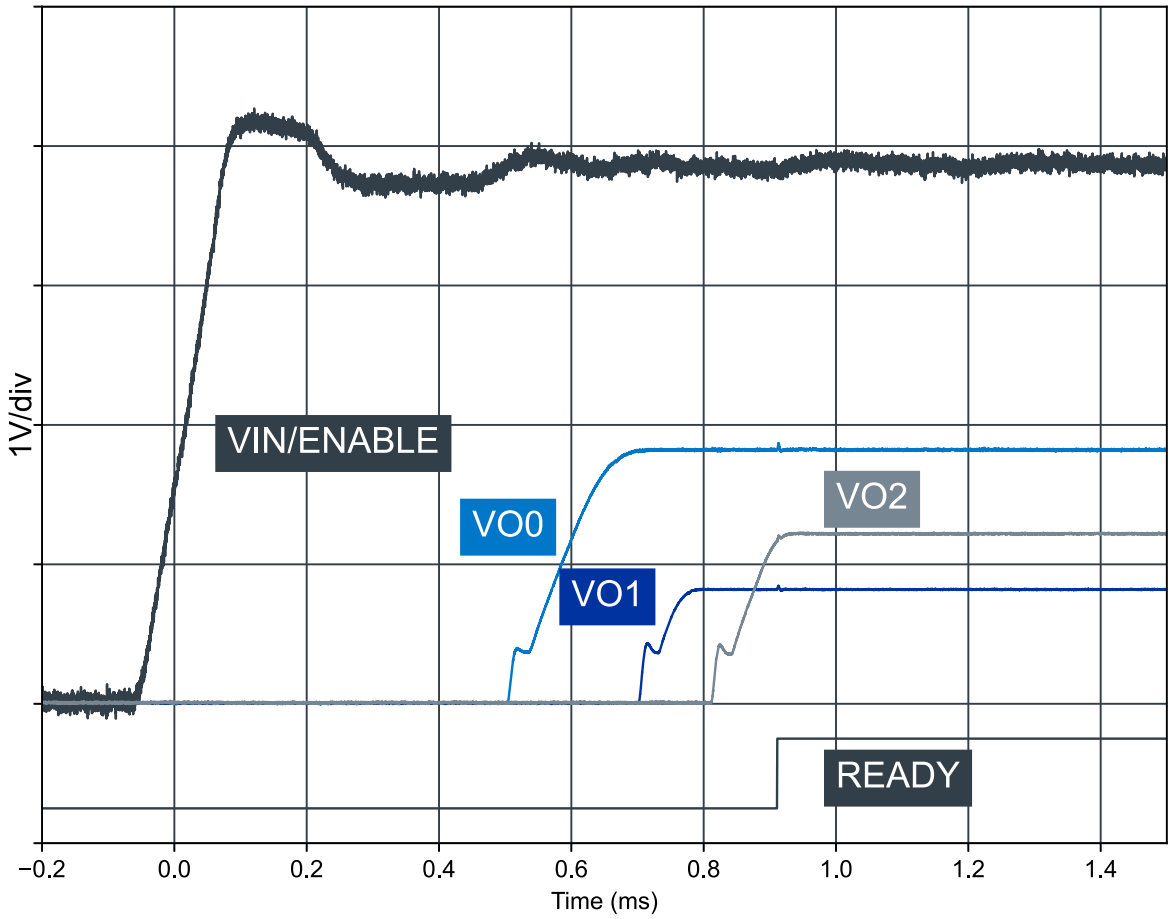


Figure 24: Start-up sequence

Designator	Value	Description	Footprint
C1, C2, C3, C4, C13, C15, C17	1 µF	Capacitor, X5R, ±10 %, 10 V	0201
C5, C6, C7, C8, C9, C10, C11, C14, C16	10 µF	Capacitor, X7T, ±20 %, 10 V	0603
C12	4.7 µF	Capacitor, X7T, ±20 %, 10 V	0603
L1, L2, L3	2.2 µH	Fixed inductor, I_{sat} > 2 A, DCR < 100 mΩ	0806
L4	470 nH	Fixed inductor, I_{sat} > 1.5 A, DCR < 100 mΩ	0603
R1, R2	10 kΩ	Resistor, ±5 %, value depends on TWI bus speed and parasitic load capacitance	0201
R3, R4	4.7 kΩ	Resistor, ±5 %, value depends on parasitic load capacitance	0201
U1	nPM6001-CAAA	Low-power and high efficiency PMIC	WLCSP-45

Table 27: Bill of material for configuration 1

8.3.2 Configuration 2

The reference schematic and bill of materials for a custom configuration are shown here.

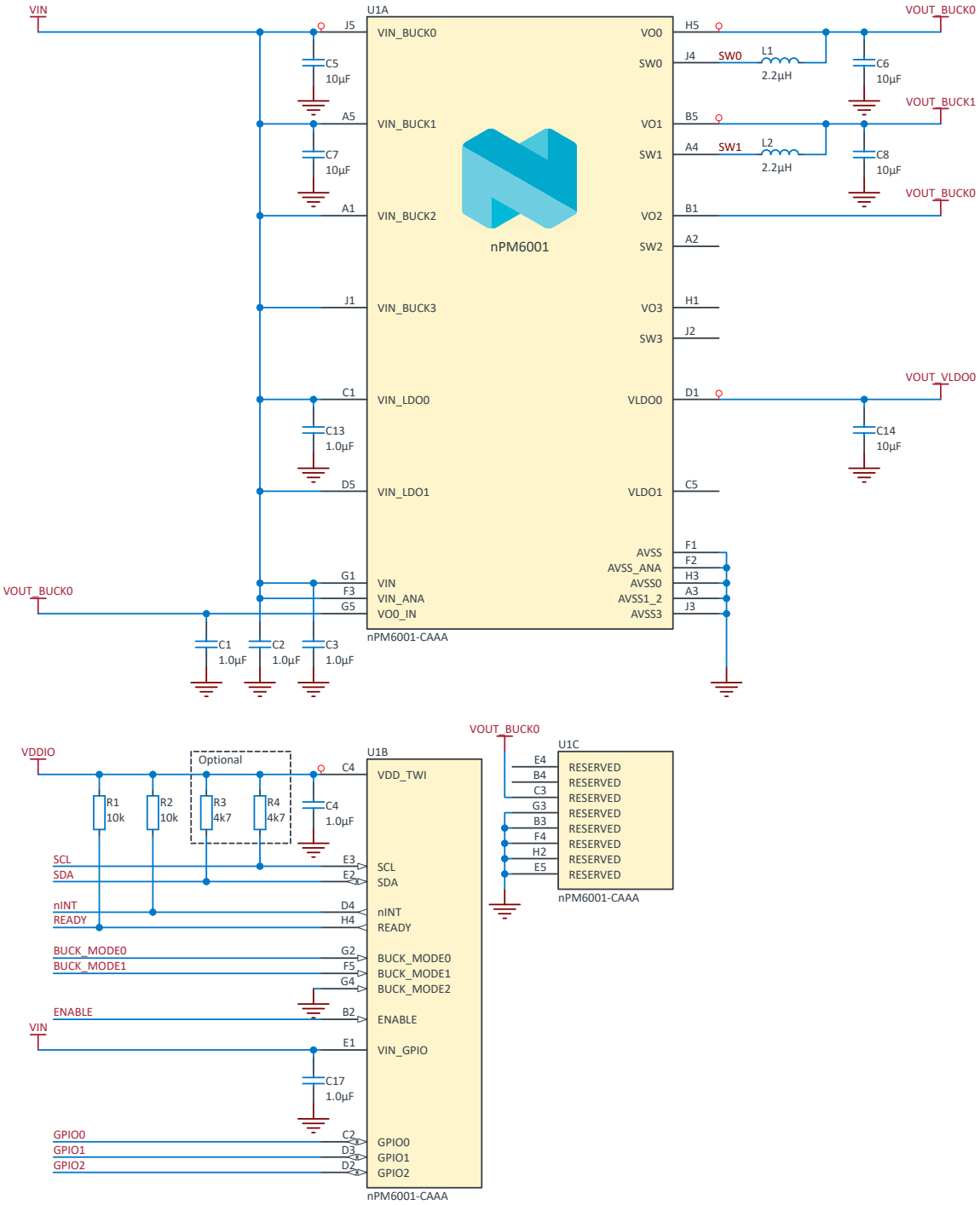


Figure 25: Reference application schematics, configuration 2

In this configuration, the unused regulators are unpopulated and must be connected as shown in the schematic. When BUCK2 is not populated, the **VO2** pin must be connected to **VO0** output for the device to operate.

The **READY** pin is set when BUCK1 starts. That means the start-up sequence does not wait for unpopulated BUCKs, but continues to the next enabled BUCK and sets the **READY** pin. To minimize power consumption, it is recommended to disable the core circuit of the unpopulated regulator BUCK2 by writing to register OVERRIDE.PWRUP.BUCK[2, 6] = [1, 0].

Designator	Value	Description	Footprint
C1, C2, C3, C4, C13, C17	1 µF	Capacitor, X5R, ±10 %, 10 V	0201
C5, C6, C7, C8, C14	10 µF	Capacitor, X7T, ±20 %, 10 V	0603
L1, L2	2.2 µH	Fixed inductor, I_{sat} > 2 A, DCR < 100 mΩ	0806
R1, R2	10 kΩ	Resistor, ±5 %, value depends on TWI bus speed and parasitic load capacitance	0201
R3, R4	4.7 kΩ	Resistor, ±5 %, value depends on parasitic load capacitance	0201
U1	nPM6001-CAAA	Low-power and high efficiency PMIC	WLCSP-45

Table 28: Bill of material for configuration 2

8.3.2.1 Electrical specification

The following table contains the Schmitt trigger mode electrical specifications for standard digital I/O driver cells used in **GPIO** and **BUCK_MODE[n]** pins in configuration 2, where **VO2** is supplied from an external source instead of BUCK2.

Symbol	Description	Min.	Typ.	Max.	Units
VT_{POS}	Positive going input voltage threshold (custom configuration **VO2**=1.8 V)	1.0		1.3	V
VT_{NEG}	Negative going input voltage threshold (custom configuration **VO2**=1.8 V)	0.6		0.7	V
D_{VT}	Hysteresis (VT_{POS} - VT_{NEG}) (custom configuration **VO2**=1.8 V)		0.5		V
VT_{POS}	Positive going input voltage threshold (custom configuration **VO2**=3.3 V)	1.7		2.1	V
VT_{NEG}	Negative going input voltage threshold (custom configuration **VO2**=3.3 V)	1		1.3	V
D_{VT}	Hysteresis (VT_{POS} - VT_{NEG}) (custom configuration **VO2**=3.3 V)		0.75		V

Table 29: Config. 2 Schmitt trigger mode electrical specification

8.3.3 Configuration 3

The reference schematic and bill of materials for a custom configuration are shown here.

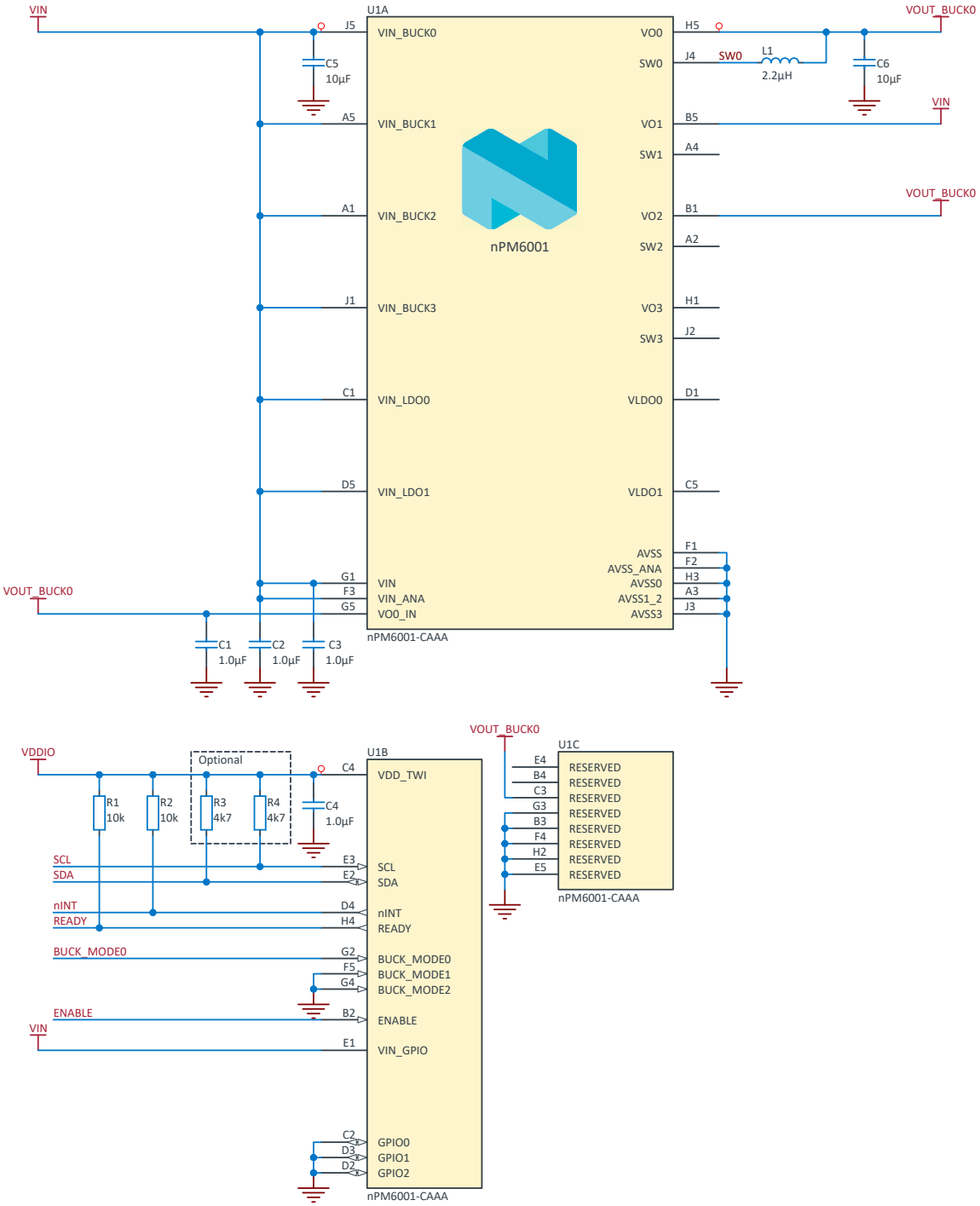


Figure 26: Reference application schematics, configuration 3

In this configuration, the unused regulators are unpopulated and must be connected as shown in the schematic. **VO1** must be connected to VIN and **VO2** must be connected to **VO0** output for the device to operate.

The **READY** pin is set when BUCK0 starts. To minimize power consumption, it is recommended to disable all core circuits of the unpopulated regulators by writing the following registers:

- Disable BUCK1 circuits – OVERRIDE.PWRUP.BUCK[1, 5] = [1, 0]
- Disable BUCK2 circuits – OVERRIDE.PWRUP.BUCK[2, 6] = [1, 0]

Unpopulated BUCK3, LDO0, and LDO1 registers do not need configuration.

Designator	Value	Description	Footprint
C1, C2, C3, C4	1 µF	Capacitor, X5R, ±10 %, 10 V	0201
C5, C6	10 µF	Capacitor, X7T, ±20 %, 10 V	0603
L1	2.2 µH	Fixed inductor, I_{sat} > 2 A, DCR < 100 mΩ	0806
R1, R2	10 kΩ	Resistor, ±5 %, value depends on TWI bus speed and parasitic load capacitance	0201
R3, R4	4.7 kΩ	Resistor, ±5 %, value depends on parasitic load capacitance	0201
U1	nPM6001-CAAA	Low-power and high efficiency PMIC	WLCSP-45

Table 30: Bill of material for configuration 3

8.3.4 PCB guidelines

A well designed PCB is necessary to achieve good performance. A poor layout can lead to loss in performance or functionality.

To ensure functionality, it is essential to follow the schematics and layout references closely.

A multilayer board with a solid ground plane is recommended for optimal performance.

The DC supply voltage should be decoupled with high performance capacitors as close as possible to the supply pins. This is important for DC/DC regulator input capacitors in order to minimize DC/DC noise levels. See the reference schematics for recommended decoupling capacitor values.

Long power supply lines on the PCB should be avoided. All device grounds, VIN and VDD connections, and bypass capacitors must be connected as close as possible to the device.

8.3.5 PCB layout example

The PCB layout shown here is a reference layout for configuration 1.

For all available reference layouts, see the Reference Layout section on the Downloads tab for nPM6001 on www.nordicsemi.com.

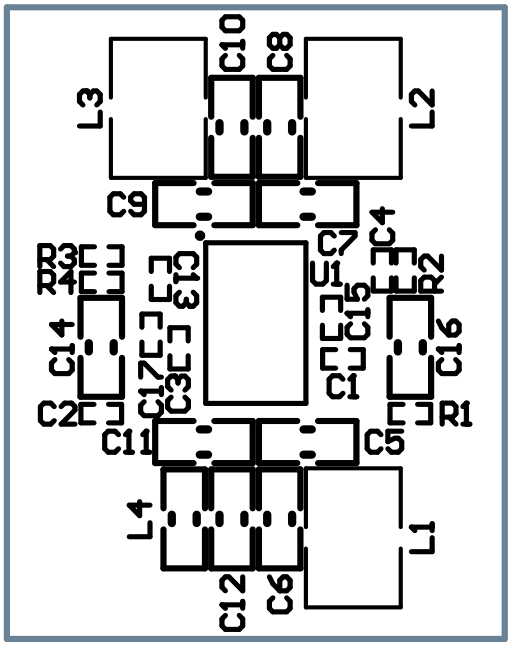


Figure 27: Top silk layer

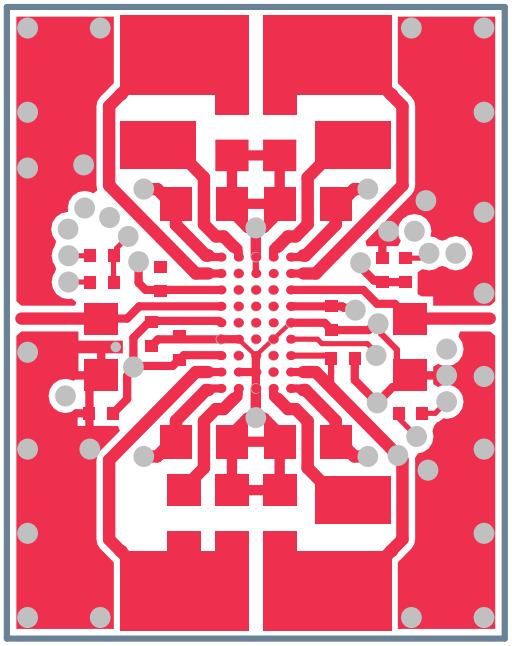


Figure 28: Top layer

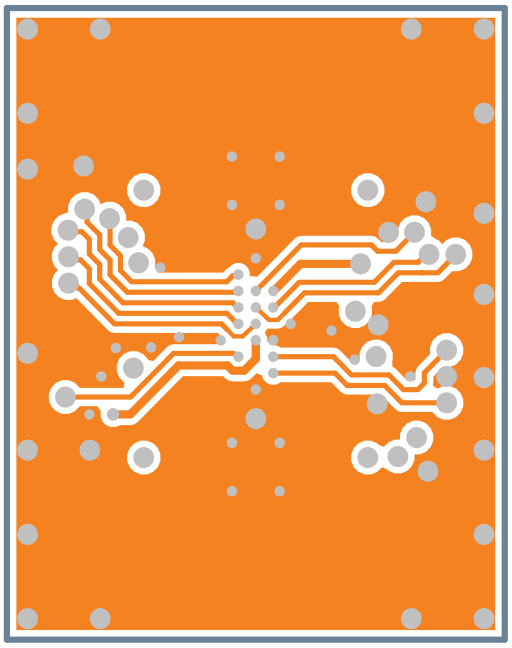


Figure 29: Inner layer 1

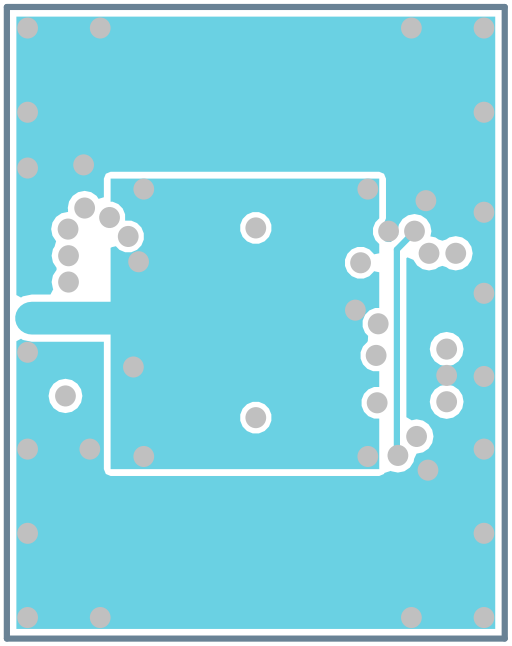


Figure 30: Inner layer 2

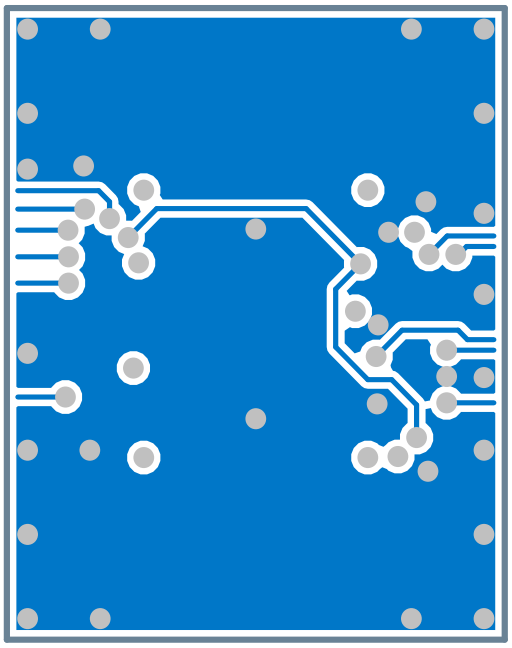


Figure 31: Bottom layer

Note: No components on the bottom layer.

9 Control and register interfaces

9.1 TWI — Two-Wire Interface

TWI is the main interface to control and monitor the device state through registers.

The following are the TWI main features:

- I2C compatible
- TWI clock 100 kHz - 400 kHz supported
- Slave device with 7-bit slave address
- Clock stretching not supported
- General Call address not supported
- Software Reset not supported
- Device ID not supported

9.2 TWI slave address

The TWI 7-bit slave-address value is 1110000b = 0x70h.

9.3 TWI electrical specification

Symbol	Description	Min.	Typ.	Max.	Units
F_SCL	Clock frequency	100		400	kHz
T_SU_DAT_100K	Data setup time before positive edge on SCL,100 kbps	250			ns
T_SU_DAT_400K	Data setup time before positive edge on SCL, 400 kbps	100			ns
T_HD_DAT	Data hold time after negative edge on SCL, all modes	0			ns
T_HD_STA_100K	Hold time from for START condition (SDA low to SCL low), 100 kbps	4000			ns
T_HD_STA_400K	Hold time from for START condition (SDA low to SCL low), 400 kbps	600			ns
T_SU_STO_100K	Setup time from SCL high to STOP condition, 100 kbps	4000			ns
T_SU_STO_400K	Setup time from SCL high to STOP condition, 400 kbps	600			ns
T_BUF_100K	Bus free time between STOP and START conditions, 100 kbps		4700		ns
T_BUF_400K	Bus free time between STOP and START conditions, 400 kbps		1300		ns

Table 31: TWI electrical specification

9.3.1 TWI timing diagram

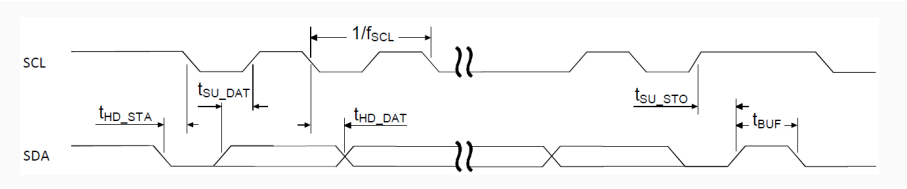


Figure 32: TWI timing diagram

9.4 Registers

Instances

Instance	Base address	Description
DIGITAL	0x00000000	nPM6001 registers

Register overview

Register	Offset	Description
SWREADY	0x01	Software ready
TASKS_START_BUCK3	0x02	Start BUCK3
TASKS_START_LDO0	0x03	Start LDO0
TASKS_START_LDO1	0x04	Start LDO1
TASKS_START_THWARN	0x06	Start thermal warning sensor
TASKS_START_TH_SHUTDN	0x07	Start thermal shutdown sensor
TASKS_STOP_BUCK3	0x08	Stop BUCK3
TASKS_STOP_LDO0	0x09	Stop LDO0
TASKS_STOP_LDO1	0x0A	Stop LDO1
TASKS_STOP_THWARN	0x0C	Stop thermal warning sensor
TASKS_STOP_THSHUTDN	0x0D	Stop thermal shutdown sensor
TASKS_UPDATE_VOUTPWM	0x0E	Update output voltage settings for BUCK0, BUCK1 and BUCK2
EVENTS_THWARN	0x1E	Thermal warning event
EVENTS_BUCK0OC	0x1F	BUCK0 overcurrent event
EVENTS_BUCK1OC	0x20	BUCK1 overcurrent event
EVENTS_BUCK2OC	0x21	BUCK2 overcurrent event
EVENTS_BUCK3OC	0x22	BUCK3 overcurrent event
INTEN0	0x2A	Enable or disable interrupts
INTENSET0	0x2B	Interrupt enable SET
INTENCLR0	0x2C	Interrupt enable CLEAR
INTPEND0	0x2D	Interrupt pending
BUCK0VOUTULP	0x3A	BUCK0 voltage setting (hysteretic mode)
BUCK0VOUTPWM	0x3B	BUCK0 voltage setting (PWM mode)
BUCK1VOUTULP	0x3C	BUCK1 voltage setting (hysteretic mode)
BUCK1VOUTPWM	0x3D	BUCK1 voltage setting (PWM mode)
BUCK2VOUTULP	0x40	BUCK2 voltage setting (hysteretic mode)
BUCK2VOUTPWM	0x41	BUCK2 voltage setting (PWM mode)
BUCK3SELDAC	0x44	Internal DAC enable for BUCK3
BUCK3VOUT	0x45	BUCK3 voltage setting
LDO0VOUT	0x46	LDO0 voltage setting
BUCK0CONFPWMMODE	0x4A	BUCK0 PWM mode configuration
BUCK1CONFPWMMODE	0x4B	BUCK1 PWM mode configuration
BUCK2CONFPWMMODE	0x4C	BUCK2 PWM mode configuration
BUCK3CONFPWMMODE	0x4D	BUCK3 PWM mode configuration
BUCKMODEPADCONF	0x4E	BUCK_MODE pin configuration
THDYNPOWERUP	0x50	Thermal sensors' dynamic configuration
PADDRIVESTRENGTH	0x53	Drive strength control
WDARMEDVALUE	0x54	Arm watchdog or wake-up timer. Use strobe WDARMEDSTROBE.
WDARMEDSTROBE	0x55	Strobe for register WDARMEDVALUE
WDTRIGGERVALUE0	0x56	Watchdog and wake-up timer trigger value, lowest byte. Use strobe WDDATASTROBE
WDTRIGGERVALUE1	0x57	Watchdog and wake-up timer trigger value, middle byte. Use strobe WDDATASTROBE
WDTRIGGERVALUE2	0x58	Watchdog and wake-up timer trigger value, highest byte. Use strobe WDDATASTROBE
WDDATASTROBE	0x5D	Strobe for registers WDTRIGGERVALUE
WDPWRUPVALUE	0x5E	Watchdog and wake-up timer enable. Use Strobe WDPWRUPSTROBE
WDPWRUPSTROBE	0x5F	Strobe for register WDPWRUPVALUE
WDKICK	0x60	Watchdog kick
WDREQPOWERDOWN	0x62	Enter hibernate mode
GPIOOUTSET	0x69	GPIO output value SET
GPIOOUTCLR	0x6A	GPIO output value CLEAR
GPIOIN	0x6B	GPIO input value
GPIO0CONF	0x6C	GPIO0 configuration

Register	Offset	Description
GPIO1CONF	0x6D	GPIO1 configuration
GPIO2CONF	0x6E	GPIO2 configuration
LDO0CTRL	0x71	LDO0 current limiter, output high-impedance and pulldown control
LDO1CTRL	0x73	LDO1 current limiter, output high-impedance and pulldown control
OVERRIDEPWRUPBUCK	0xAB	Override for disabling BUCK1 or/and BUCK2 regulators

9.4.1 SWREADY

Address offset: 0x01

Software ready

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	SWREADY			Before this bit is set, nPM6001 does not react to BUCK_MODEx pins.								
			NOTREADY	0	Software configuration is not yet done. BUCKs are running in PWM mode.								
			READY	1	Software configuration is ready. Pins BUCK_MODEx may be used to control BUCKs' PWM modes.								

9.4.2 TASKS_START_BUCK3

Address offset: 0x02

Start BUCK3

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKS_START_BUCK3			Start BUCK3								
			Trigger	1	Trigger task								

9.4.3 TASKS_START_LDO0

Address offset: 0x03

Start LDO0

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKS_START_LDO0			Start LDO0								
			Trigger	1	Trigger task								

9.4.4 TASKS_START_LDO1

Address offset: 0x04

Start LDO1

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKS_START_LDO1			Start LDO1								
			Trigger	1	Trigger task								

9.4.5 TASKS_START_THWARN

Address offset: 0x06

Start thermal warning sensor

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKS_START_THWARN			Start thermal warning sensor								
			Trigger	1	Trigger task								

9.4.6 TASKS_START_TH_SHUTDN

Address offset: 0x07

Start thermal shutdown sensor

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKS_START_TH_SHUTDN			Start thermal shutdown sensor								
			Trigger	1	Trigger task								

9.4.7 TASKS_STOP_BUCK3

Address offset: 0x08

Stop BUCK3

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKS_STOP_BUCK3			Stop BUCK3								
			Trigger	1	Trigger task								

9.4.8 TASKS_STOP_LDO0

Address offset: 0x09

Stop LDO0

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKS_STOP_LDO0			Stop LDO0								
			Trigger	1	Trigger task								

9.4.9 TASKS_STOP_LDO1

Address offset: 0x0A

Stop LDO1

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKS_STOP_LDO1			Stop LDO1								
			Trigger	1	Trigger task								

9.4.10 TASKS_STOP_THWARN

Address offset: 0x0C

Stop thermal warning sensor

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKS_STOP_THWARN			Stop thermal warning sensor								
			Trigger	1	Trigger task								

9.4.11 TASKS_STOP_THSHUTDN

Address offset: 0x0D

Stop thermal shutdown sensor

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKS_STOP_THSHUTDN			Stop thermal shutdown sensor								
			Trigger	1	Trigger task								

9.4.12 TASKS_UPDATE_VOUTPWM

Address offset: 0x0E

Update output voltage settings for BUCK0, BUCK1 and BUCK2

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	W	TASKS_UPDATE_VOUTPWM			Update output voltage settings for BUCK0, BUCK1 and BUCK2							
			Trigger	1	Trigger task							

9.4.13 EVENTS_THWARN

Address offset: 0x1E

Thermal warning event

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	EVENTS_THWARN			Thermal warning event							
			NotGenerated	0	Event not generated							
			Generated	1	Event generated							

9.4.14 EVENTS_BUCK0OC

Address offset: 0x1F

BUCK0 overcurrent event

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	EVENTS_BUCK0OC			BUCK0 overcurrent event							
			NotGenerated	0	Event not generated							
			Generated	1	Event generated							

9.4.15 EVENTS_BUCK1OC

Address offset: 0x20

BUCK1 overcurrent event

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	EVENTS_BUCK1OC			BUCK1 overcurrent event							
			NotGenerated	0	Event not generated							
			Generated	1	Event generated							

9.4.16 EVENTS_BUCK2OC

Address offset: 0x21

BUCK2 overcurrent event

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	EVENTS_BUCK2OC			BUCK2 overcurrent event							
			NotGenerated	0	Event not generated							
			Generated	1	Event generated							

9.4.17 EVENTS_BUCK3OC

Address offset: 0x22

BUCK3 overcurrent event

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	EVENTS_BUCK3OC			BUCK3 overcurrent event							
			NotGenerated	0	Event not generated							
			Generated	1	Event generated							

9.4.18 INTEN0

Address offset: 0x2A

Enable or disable interrupts

Bit number					7	6	5	4	3	2	1	0
ID					H	G	F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	RESERVED0			Reserved0. Do not write '1' to bits marked as RESERVEDn.							
B	RW	RESERVED1			Reserved1. Do not write '1' to bits marked as RESERVEDn.							
C	RW	RESERVED2			Reserved2. Do not write '1' to bits marked as RESERVEDn.							
D	RW	THWARN			Enable or disable interrupt for event thermal warning							
			DISABLED	0	Disable							
			ENABLED	1	Enable							
E	RW	BUCK0OC			Enable or disable interrupt for event BUCK0 overcurrent							
			DISABLED	0	Disable							
			ENABLED	1	Enable							
F	RW	BUCK1OC			Enable or disable interrupt for event BUCK1 overcurrent							
			DISABLED	0	Disable							
			ENABLED	1	Enable							
G	RW	BUCK2OC			Enable or disable interrupt for event BUCK2 overcurrent							
			DISABLED	0	Disable							
			ENABLED	1	Enable							
H	RW	BUCK3OC			Enable or disable interrupt for event BUCK3 overcurrent							
			DISABLED	0	Disable							
			ENABLED	1	Enable							

9.4.19 INTENSET0

Address offset: 0x2B

Interrupt enable SET

Bit number					7	6	5	4	3	2	1	0
ID					H	G	F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1S	RESERVED0			Reserved0. Do not write '1' to bits marked as RESERVEDn.							
B	RW W1S	RESERVED1			Reserved1. Do not write '1' to bits marked as RESERVEDn.							
C	RW W1S	RESERVED2			Reserved2. Do not write '1' to bits marked as RESERVEDn.							
D	RW W1S	THWARN			Thermal warning							
			NOACTION	0	No Action							
			SET	1	Set							
E	RW W1S	BUCK0OC			BUCK0 overcurrent							
			NOACTION	0	No Action							
			SET	1	Set							
F	RW W1S	BUCK1OC			BUCK1 overcurrent							
			NOACTION	0	No Action							
			SET	1	Set							
G	RW W1S	BUCK2OC			BUCK2 overcurrent							
			NOACTION	0	No Action							
			SET	1	Set							
H	RW W1S	BUCK3OC			BUCK3 overcurrent							
			NOACTION	0	No Action							
			SET	1	Set							

9.4.20 INTENCLR0

Address offset: 0x2C

Interrupt enable CLEAR

Bit number					7	6	5	4	3	2	1	0
ID					H	G	F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1C	RESERVED0			Reserved0. Do not write '1' to bits marked as RESERVEDn.							
B	RW W1C	RESERVED1			Reserved1. Do not write '1' to bits marked as RESERVEDn.							
C	RW W1C	RESERVED2			Reserved2. Do not write '1' to bits marked as RESERVEDn.							
D	RW W1C	THWARN			Thermal warning							
			NOACTION	0	No Action							
			CLEAR	1	Clear							

Bit number					7	6	5	4	3	2	1	0
ID					H	G	F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
E	RW W1C	BUCK0OC			BUCK0 overcurrent							
			NOACTION	0	No Action							
			CLEAR	1	Clear							
F	RW W1C	BUCK1OC			BUCK1 overcurrent							
			NOACTION	0	No Action							
			CLEAR	1	Clear							
G	RW W1C	BUCK2OC			BUCK2 overcurrent							
			NOACTION	0	No Action							
			CLEAR	1	Clear							
H	RW W1C	BUCK3OC			BUCK3 overcurrent							
			NOACTION	0	No Action							
			CLEAR	1	Clear							

9.4.21 INTPEND0

Address offset: 0x2D

Interrupt pending

Bit number					7	6	5	4	3	2	1	0
ID					H	G	F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	R	RESERVED0			Reserved0. Do not write '1' to bits marked as RESERVEDn.							
B	R	RESERVED1			Reserved1. Do not write '1' to bits marked as RESERVEDn.							
C	R	RESERVED2			Reserved2. Do not write '1' to bits marked as RESERVEDn.							
D	R	THWARN			Thermal warning							
			NOTPENDING	0	Not Pending							
			PENDING	1	Pending							
E	R	BUCK0OC			BUCK0 overcurrent							
			NOTPENDING	0	Not Pending							
			PENDING	1	Pending							
F	R	BUCK1OC			BUCK1 overcurrent							
			NOTPENDING	0	Not Pending							
			PENDING	1	Pending							
G	R	BUCK2OC			BUCK2 overcurrent							
			NOTPENDING	0	Not Pending							
			PENDING	1	Pending							
H	R	BUCK3OC			BUCK3 overcurrent							
			NOTPENDING	0	Not Pending							
			PENDING	1	Pending							

9.4.22 BUCK0VOUTULP

Address offset: 0x3A

BUCK0 voltage setting (hysteretic mode)

Bit number					7	6	5	4	3	2	1	0
ID								B	A	A	A	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	VOLTAGE			BUCK0 voltage setting for hysteretic mode. Setting must be identical with register BUCK0VOUTPWM.							
			SET1V8	0	SET 1V8							
			SET1V9	1	SET 1V9							
			SET2V0	2	SET 2V0							
			SET2V1	3	SET 2V1							
			SET2V2	4	SET 2V2							
			SET2V3	5	SET 2V3							
			SET2V4	6	SET 2V4							
			SET2V5	7	SET 2V5							
			SET2V6	8	SET 2V6							
			SET2V7	9	SET 2V7							
			SET2V8	10	SET 2V8							
			SET2V9	11	SET 2V9							
			SET3V0	12	SET 3V0							
			SET3V1	13	SET 3V1							
			SET3V2	14	SET 3V2							
			SET3V3	15	SET 3V3							
B	RW	RESERVED0			Reserved0. Do not write '1' to bits marked as RESERVEDn.							

9.4.23 BUCK0VOUTPWM

Address offset: 0x3B

BUCK0 voltage setting (PWM mode)

Bit number					7	6	5	4	3	2	1	0
ID								B	A	A	A	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	VOLTAGE			BUCK0 voltage setting for PWM mode. After updating this register, run TASK_UPDATE_VOUTPWM.							
			SET1V8	0	SET 1V8							
			SET1V9	1	SET 1V9							
			SET2V0	2	SET 2V0							
			SET2V1	3	SET 2V1							
			SET2V2	4	SET 2V2							
			SET2V3	5	SET 2V3							
			SET2V4	6	SET 2V4							
			SET2V5	7	SET 2V5							
			SET2V6	8	SET 2V6							
			SET2V7	9	SET 2V7							
			SET2V8	10	SET 2V8							
			SET2V9	11	SET 2V9							
			SET3V0	12	SET 3V0							
			SET3V1	13	SET 3V1							
			SET3V2	14	SET 3V2							
			SET3V3	15	SET 3V3							
B	RW	RESERVED0			Reserved0. Do not write '1' to bits marked as RESERVEDn.							

9.4.24 BUCK1VOUTULP

Address offset: 0x3C

BUCK1 voltage setting (hysteretic mode)

Bit number					7	6	5	4	3	2	1	0
ID								B	A	A	A	A
Reset 0x02					**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	VOLTAGE			BUCK1 voltage setting for hysteretic mode. Setting must be identical with register BUCK1VOUTPWM.							
			SET0V70	0	SET 0V70							
			SET0V75	1	SET 0V75							
			SET0V80	2	SET 0V80							
			SET0V85	3	SET 0V85							
			SET0V90	4	SET 0V90							
			SET0V95	5	SET 0V95							
			SET1V00	6	SET 1V00							
			SET1V05	7	SET 1V05							
			SET1V10	8	SET 1V10							
			SET1V15	9	SET 1V15							
			SET1V20	10	SET 1V20							
			SET1V25	11	SET 1V25							
			SET1V30	12	SET 1V30							
			SET1V35	13	SET 1V35							
			SET1V40	14	SET 1V40							
B	RW	RESERVED0			Reserved0. Do not write '1' to bits marked as RESERVEDn.							

9.4.25 BUCK1VOUTPWM

Address offset: 0x3D

BUCK1 voltage setting (PWM mode)

Bit number					7	6	5	4	3	2	1	0
ID								B	A	A	A	A
Reset 0x02					**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	VOLTAGE			BUCK1 voltage setting for PWM mode. After updating this register, run TASK_UPDATE_VOUTPWM							
			SET0V70	0	SET 0V70							
			SET0V75	1	SET 0V75							
			SET0V80	2	SET 0V80							
			SET0V85	3	SET 0V85							
			SET0V90	4	SET 0V90							
			SET0V95	5	SET 0V95							
			SET1V00	6	SET 1V00							
			SET1V05	7	SET 1V05							
			SET1V10	8	SET 1V10							
			SET1V15	9	SET 1V15							
			SET1V20	10	SET 1V20							
			SET1V25	11	SET 1V25							
			SET1V30	12	SET 1V30							

Bit number					7	6	5	4	3	2	1	0
ID								B	A	A	A	A
Reset 0x02					**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
ID	R/W	Field	Value ID	Value	Description							
			SET1V35	13	SET 1V35							
			SET1V40	14	SET 1V40							
B	RW	RESERVED0			Reserved0. Do not write '1' to bits marked as RESERVEDn.							

9.4.26 BUCK2VOUTULP

Address offset: 0x40

BUCK2 voltage setting (hysteretic mode)

Bit number					7	6	5	4	3	2	1	0
ID								A	A	A	A	A
Reset 0x0A					**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	VOLTAGE			BUCK2 voltage setting for hysteretic mode. Setting must be identical with register BUCK2VOUTPWM.							
			SET1V20	10	SET 1V20							
			SET1V25	11	SET 1V25							
			SET1V30	12	SET 1V30							
			SET1V35	13	SET 1V35							
			SET1V40	14	SET 1V40							

9.4.27 BUCK2VOUTPWM

Address offset: 0x41

BUCK2 voltage setting (PWM mode)

Bit number					7	6	5	4	3	2	1	0
ID								A	A	A	A	A
Reset 0x0A					**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	VOLTAGE			BUCK2 voltage setting for PWM-mode. After updating this register, run TASK_UPDATE_VOUTPWM.							
			SET1V20	10	SET 1V20							
			SET1V25	11	SET 1V25							
			SET1V30	12	SET 1V30							
			SET1V35	13	SET 1V35							
			SET1V40	14	SET 1V40							

9.4.28 BUCK3SELDAC

Address offset: 0x44

Internal DAC enable for BUCK3

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	SELECT			BUCK3 internal DAC								
			DISABLE	0	Disable								
			ENABLE	1	Enable								

9.4.29 BUCK3VOUT

Address offset: 0x45

BUCK3 voltage setting

Bit number						7	6	5	4	3	2	1	0
ID							A	A	A	A	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	VOLTAGE			BUCK3 voltage setting								
			SET0V5	0	SET 0V5								
			SET0V525	1	SET 0V525								
			SET0V55	2	SET 0V55								
			SET0V575	3	SET 0V575								
			SET0V6	4	SET 0V6								
			SET0V625	5	SET 0V625								
			SET0V65	6	SET 0V65								
			SET0V675	7	SET 0V675								
			SET0V7	8	SET 0V7								
			SET0V725	9	SET 0V725								
			SET0V75	10	SET 0V75								
			SET0V775	11	SET 0V775								
			SET0V8	12	SET 0V8								
			SET0V825	13	SET 0V825								
			SET0V85	14	SET 0V85								
			SET0V875	15	SET 0V875								
			SET0V9	16	SET 0V9								
			SET0V925	17	SET 0V925								
			SET0V95	18	SET 0V95								
			SET0V975	19	SET 0V975								
			SET1V0	20	SET 1V0								
			SET1V025	21	SET 1V025								
			SET1V05	22	SET 1V05								
			SET1V075	23	SET 1V075								
			SET1V1	24	SET 1V1								
			SET1V125	25	SET 1V125								
			SET1V15	26	SET 1V15								
			SET1V175	27	SET 1V175								
			SET1V2	28	SET 1V2								
			SET1V225	29	SET 1V225								
			SET1V25	30	SET 1V25								
			SET1V275	31	SET 1V275								
			SET1V3	32	SET 1V3								
			SET1V325	33	SET 1V325								
			SET1V35	34	SET 1V35								

Bit number						7	6	5	4	3	2	1	0
ID							A	A	A	A	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
			SET1V375	35	SET 1V375								
			SET1V4	36	SET 1V4								
			SET1V425	37	SET 1V425								
			SET1V45	38	SET 1V45								
			SET1V475	39	SET 1V475								
			SET1V5	40	SET 1V5								
			SET1V525	41	SET 1V525								
			SET1V55	42	SET 1V55								
			SET1V575	43	SET 1V575								
			SET1V6	44	SET 1V6								
			SET1V625	45	SET 1V625								
			SET1V65	46	SET 1V65								
			SET1V675	47	SET 1V675								
			SET1V7	48	SET 1V7								
			SET1V725	49	SET 1V725								
			SET1V75	50	SET 1V75								
			SET1V775	51	SET 1V775								
			SET1V8	52	SET 1V8								
			SET1V825	53	SET 1V825								
			SET1V85	54	SET 1V85								
			SET1V875	55	SET 1V875								
			SET1V9	56	SET 1V9								
			SET1V925	57	SET 1V925								
			SET1V95	58	SET 1V95								
			SET1V975	59	SET 1V975								
			SET2V0	60	SET 2V0								
			SET2V025	61	SET 2V025								
			SET2V05	62	SET 2V05								
			SET2V075	63	SET 2V075								
			SET2V1	64	SET 2V1								
			SET2V125	65	SET 2V125								
			SET2V15	66	SET 2V15								
			SET2V175	67	SET 2V175								
			SET2V2	68	SET 2V2								
			SET2V225	69	SET 2V225								
			SET2V25	70	SET 2V25								
			SET2V275	71	SET 2V275								
			SET2V3	72	SET 2V3								
			SET2V325	73	SET 2V325								
			SET2V35	74	SET 2V35								
			SET2V375	75	SET 2V375								
			SET2V4	76	SET 2V4								
			SET2V425	77	SET 2V425								
			SET2V45	78	SET 2V45								
			SET2V475	79	SET 2V475								
			SET2V5	80	SET 2V5								
			SET2V525	81	SET 2V525								
			SET2V55	82	SET 2V55								
			SET2V575	83	SET 2V575								
			SET2V6	84	SET 2V6								

Bit number						7	6	5	4	3	2	1	0
ID							A	A	A	A	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
			SET2V625	85	SET 2V625								
			SET2V65	86	SET 2V65								
			SET2V675	87	SET 2V675								
			SET2V7	88	SET 2V7								
			SET2V725	89	SET 2V725								
			SET2V75	90	SET 2V75								
			SET2V775	91	SET 2V775								
			SET2V8	92	SET 2V8								
			SET2V825	93	SET 2V825								
			SET2V85	94	SET 2V85								
			SET2V875	95	SET 2V875								
			SET2V9	96	SET 2V9								
			SET2V925	97	SET 2V925								
			SET2V95	98	SET 2V95								
			SET2V975	99	SET 2V975								
			SET3V0	100	SET 3V0								
			SET3V025	101	SET 3V025								
			SET3V05	102	SET 3V05								
			SET3V075	103	SET 3V075								
			SET3V1	104	SET 3V1								
			SET3V125	105	SET 3V125								
			SET3V15	106	SET 3V15								
			SET3V175	107	SET 3V175								
			SET3V2	108	SET 3V2								
			SET3V225	109	SET 3V225								
			SET3V25	110	SET 3V25								
			SET3V275	111	SET 3V275								
			SET3V3	112	SET 3V3								

9.4.30 LDO0VOUT

Address offset: 0x46

LDO0 voltage setting

Bit number						7	6	5	4	3	2	1	0
ID							B	A	A	A	A	A	A
Reset 0x1A						**0**	**0**	**0**	**1**	**1**	**0**	**1**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	VOLTAGE			LDO0 voltage setting								
			SET1V8	6	SET 1.8V								
			SET2V1	11	SET 2.1V								
			SET2V41	16	SET 2.41V								
			SET2V7	21	SET 2.7V								
			SET3V0	26	SET 3.0V								
			SET3V3	30	SET 3.3V								
B	RW	RESERVED0			Reserved0. Do not write '1' to bits marked as RESERVEDn.								

9.4.31 BUCK0CONFPWMMODE

Address offset: 0x4A

BUCK0 PWM mode configuration

Bit number					7	6	5	4	3	2	1	0
ID									D	C	B	A
Reset 0x03					**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**
ID	R/W	Field	Value ID	Value	Description							
A	RW	PADBUCKMODE0			Configure pin BUCK_MODE0 for BUCK0							
			NOPWM	0	BUCK0 is not set to PWM mode when pin BUCK_MODE0 is high							
			PWM	1	BUCK0 is set to PWM mode when pin BUCK_MODE0 is high							
B	RW	PADBUCKMODE1			Configure pin BUCK_MODE1 for BUCK0							
			NOPWM	0	BUCK0 is not set to PWM mode when pin BUCK_MODE1 is high							
			PWM	1	BUCK0 is set to PWM mode when pin BUCK_MODE1 is high							
C	RW	PADBUCKMODE2			Configure pin BUCK_MODE2 for BUCK0							
			NOPWM	0	BUCK0 is not set to PWM mode when pin BUCK_MODE2 is high							
			PWM	1	BUCK0 is set to PWM mode when pin BUCK_MODE2 is high							
D	RW	SETFORCEPWM			Set BUCK0 to PWM mode							
			OFF	0	BUCK0 PWM mode is controlled by BUCK_MODE pins							
			ON	1	BUCK0 is set to PWM mode regardless of BUCK_MODE pin states							

9.4.32 BUCK1CONFPWMMODE

Address offset: 0x4B

BUCK1 PWM mode configuration

Bit number					7	6	5	4	3	2	1	0
ID									D	C	B	A
Reset 0x02					**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	PADBUCKMODE0			Configure pin BUCK_MODE0 for BUCK1							
			NOPWM	0	BUCK1 is not set to PWM mode when pin BUCK_MODE0 is high							
			PWM	1	BUCK1 is set to PWM mode when pin BUCK_MODE0 is high							
B	RW	PADBUCKMODE1			Configure pin BUCK_MODE1 for BUCK1							
			NOPWM	0	BUCK1 is not set to PWM mode when pin BUCK_MODE1 is high							
			PWM	1	BUCK1 is set to PWM mode when pin BUCK_MODE1 is high							
C	RW	PADBUCKMODE2			Configure pin BUCK_MODE2 for BUCK1							
			NOPWM	0	BUCK1 is not set to PWM mode when pin BUCK_MODE2 is high							
			PWM	1	BUCK1 is set to PWM mode when pin BUCK_MODE2 is high							
D	RW	SETFORCEPWM			Set BUCK1 to PWM mode							
			OFF	0	BUCK1 PWM mode is controlled by BUCK_MODE pins							
			ON	1	BUCK1 is set to PWM mode regardless of BUCK_MODE pin states							

9.4.33 BUCK2CONFPWMMODE

Address offset: 0x4C

BUCK2 PWM mode configuration

Bit number					7	6	5	4	3	2	1	0
ID									D	C	B	A
Reset 0x02					**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	PADBUCKMODE0			Configure pin BUCK_MODE0 for BUCK2							
			NOPWM	0	BUCK2 is not set to PWM mode when pin BUCK_MODE0 is high							
			PWM	1	BUCK2 set to PWM mode when pin BUCK_MODE0 is high							
B	RW	PADBUCKMODE1			Configure pin BUCK_MODE1 for BUCK2							
			NOPWM	0	BUCK2 is not set to PWM mode when pin BUCK_MODE1 is high							
			PWM	1	BUCK2 is set to PWM mode when pin BUCK_MODE1 is high							
C	RW	PADBUCKMODE2			Configure pin BUCK_MODE2 for BUCK2							
			NOPWM	0	BUCK2 is not set to PWM mode when pin BUCK_MODE2 is high							
			PWM	1	BUCK2 is set to PWM mode when pin BUCK_MODE2 is high							
D	RW	SETFORCEPWM			Set BUCK2 to PWM mode							
			OFF	0	BUCK2 PWM mode is controlled by BUCK_MODE pins							
			ON	1	BUCK2 is set to PWM mode regardless of BUCK_MODE pin states							

9.4.34 BUCK3CONFPWMMODE

Address offset: 0x4D

BUCK3 PWM mode configuration

Bit number					7	6	5	4	3	2	1	0
ID									D	C	B	A
Reset 0x04					**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	PADBUCKMODE0			Configure pin BUCK_MODE0 for BUCK3							
			NOPWM	0	BUCK3 is not set to PWM mode when pin BUCK_MODE0 is high							
			PWM	1	BUCK3 is set to PWM mode when pin BUCK_MODE0 is high							
B	RW	PADBUCKMODE1			Configure pin BUCK_MODE1 for BUCK3							
			NOPWM	0	BUCK3 is not set to PWM mode when pin BUCK_MODE1 is high							
			PWM	1	BUCK3 is set to PWM mode when pin BUCK_MODE1 is high							
C	RW	PADBUCKMODE2			Configure pin BUCK_MODE2 for BUCK3							
			NOPWM	0	BUCK3 is not set to PWM mode when pin BUCK_MODE2 is high							
			PWM	1	BUCK3 is set to PWM mode when pin BUCK_MODE2 is high							
D	RW	SETFORCEPWM			Set BUCK3 to PWM mode							
			OFF	0	BUCK3 PWM mode is controlled by BUCK_MODE pins							
			ON	1	BUCK3 is set to PWM mode regardless of BUCK_MODE pin states							

9.4.35 BUCKMODEPADCONF

Address offset: 0x4E

BUCK_MODE pin configuration

Bit number					7	6	5	4	3	2	1	0
ID						F	E	D		C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	BUCKMODE0PADTYPE			BUCK_MODE0 input type							
			SCHMITT	0	Schmitt trigger input							
			CMOS	1	CMOS input							
B	RW	BUCKMODE1PADTYP			BUCK_MODE1 input type							

Bit number						7	6	5	4	3	2	1	0
ID							F	E	D		C	B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
			SCHMITT	0	Schmitt trigger input								
			CMOS	1	CMOS input								
C	RW	BUCKMODE2PADTYPE			BUCK_MODE2 input type								
			SCHMITT	0	Schmitt trigger input								
			CMOS	1	CMOS input								
D	RW	BUCKMODE0PULLD			BUCK_MODE0 pulldown								
			DISABLED	0	Disabled								
			ENABLED	1	Enabled								
E	RW	BUCKMODE1PULLD			BUCK_MODE1 pulldown								
			DISABLED	0	Disabled								
			ENABLED	1	Enabled								
F	RW	BUCKMODE2PULLD			BUCK_MODE2 pulldown								
			DISABLED	0	Disabled								
			ENABLED	1	Enabled								

9.4.36 THDYNPOWERUP

Address offset: 0x50

Thermal sensors' dynamic configuration

Bit number						7	6	5	4	3	2	1	0
ID								F	E	D	C	B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	BUCK0PWM			BUCK0 PWM mode controls thermal sensor								
			NOEFFECT	0	Thermal sensor is not enabled while BUCK0 is in PWM mode								
			PWRUP	1	Thermal sensor is enabled while BUCK0 is in PWM mode								
B	RW	BUCK1PWM			BUCK1 PWM mode controls thermal sensor								
			NOEFFECT	0	Thermal sensor is not enabled while BUCK1 is in PWM mode								
			PWRUP	1	Thermal sensor is enabled while BUCK1 is in PWM mode								
C	RW	BUCK2PWM			BUCK2 PWM mode controls thermal sensor								
			NOEFFECT	0	Thermal sensor is not enabled while BUCK2 is in PWM mode								
			PWRUP	1	Thermal sensor is enabled while BUCK2 is in PWM mode								
D	RW	BUCK3PWM			BUCK3 PWM mode controls thermal sensor								
			NOEFFECT	0	Thermal sensor is not enabled while BUCK3 is in PWM mode								
			PWRUP	1	Thermal sensor is enabled while BUCK3 is in PWM mode								
E	RW	WARNING			Thermal warning sensor								
			NOTSELECTED	0	Thermal warning sensor is not enabled dynamically								
			SELECTED	1	Thermal warning sensor is enabled dynamically								
F	RW	SHUTDWN			Thermal shutdown sensor								
			NOTSELECTED	0	Thermal shutdown sensor is not enabled dynamically								
			SELECTED	1	Thermal shutdown sensor is enabled dynamically								

9.4.37 PADDRIVESTRENGTH

Address offset: 0x53

Drive strength control

Bit number					7	6	5	4	3	2	1	0
ID						G	F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	RESERVED0			Reserved0. Do not write '1' to bits marked as RESERVEDn.							
B	RW	RESERVED1			Reserved1. Do not write '1' to bits marked as RESERVEDn.							
C	RW	READY			Drive strength for pin READY							
			NORMAL	0	Normal drive strength							
			HIGH	1	High drive strength							
D	RW	NINT			Drive strength for pin nINT							
			NORMAL	0	Normal drive strength							
			HIGH	1	High drive strength							
E	RW	RESERVED2			Reserved2. Do not write '1' to bits marked as RESERVEDn.							
F	RW	SDA			Drive strength for pin SDA							
			NORMAL	0	Normal drive strength							
			HIGH	1	High drive strength							
G	RW	RESERVED3			Reserved3. Do not write '1' to bits marked as RESERVEDn.							

9.4.38 WDARMEDVALUE

Address offset: 0x54

Arm watchdog or wake-up timer. Use strobe WDARMEDSTROBE.

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	VALUE			Arm or disarm watchdog or wake-up timer							
			DISABLE	0	Disarmed							
			ENABLE	1	Armed							

9.4.39 WDARMEDSTROBE

Address offset: 0x55

Strobe for register WDARMEDVALUE

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	W	STROBE			Strobe for register WDARMEDVALUE							
			NOEFFECT	0	No effect							
			STROBE	1	Strobe							

9.4.40 WDTRIGGERVALUE0

Address offset: 0x56

Watchdog and wake-up timer trigger value, lowest byte. Use strobe WDDATASTROBE

Bit number					7	6	5	4	3	2	1	0
ID					A	A	A	A	A	A	A	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	VALUE0			Watchdog and wakeup timer trigger value is a 24-bit value programmed into three registers. This is the lowest byte. Lsb equals to 4 s. Do not use values 0 and 1.							
			SEL0	0	Sel0							
			SEL2	2	Sel2							
			SEL3	3	Sel3							
			SEL4	4	Sel4							
			SEL5	5	Sel5							
			SEL6	6	Sel6							
			SEL7	7	Sel7							
			SEL8	8	Sel8							
			SEL16	16	Sel16							
			SEL32	32	Sel32							
			SEL64	64	Sel64							
			SEL128	128	Sel128							

9.4.41 WDTRIGGERVALUE1

Address offset: 0x57

Watchdog and wake-up timer trigger value, middle byte. Use strobe WDDATASTROBE

Bit number					7	6	5	4	3	2	1	0
ID					A	A	A	A	A	A	A	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	VALUE1			Watchdog and wakeup timer trigger value, middle byte.							
			SEL0	0	Sel0							
			SEL1	1	Sel1							
			SEL2	2	Sel2							
			SEL4	4	Sel4							
			SEL8	8	Sel8							
			SEL16	16	Sel16							
			SEL32	32	Sel32							
			SEL64	64	Sel64							
			SEL128	128	Sel128							

9.4.42 WDTRIGGERVALUE2

Address offset: 0x58

Watchdog and wake-up timer trigger value, highest byte. Use strobe WDDATASTROBE

Bit number					7	6	5	4	3	2	1	0
ID					A	A	A	A	A	A	A	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	VALUE2			Watchdog and wakeup timer trigger value, highest byte.							
			SEL0	0	Sel0							
			SEL1	1	Sel1							
			SEL2	2	Sel2							
			SEL4	4	Sel4							
			SEL8	8	Sel8							
			SEL16	16	Sel16							
			SEL32	32	Sel32							
			SEL64	64	Sel64							
			SEL128	128	Sel128							

9.4.43 WDDATASTROBE

Address offset: 0x5D

Strobe for registers WDTRIGGERVALUE

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	W	STROBE			Strobe for registers WDTRIGGERVALUEx							
			NOEFFECT	0	No effect							
			STROBE	1	Strobe							

9.4.44 WDPWRUPVALUE

Address offset: 0x5E

Watchdog and wake-up timer enable. Use Strobe WDPWRUPSTROBE

Bit number					7	6	5	4	3	2	1	0
ID										C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	OSC			Oscillator enable for watchdog and wake-up timer							
			DISABLE	0	Disable							
			ENABLE	1	Enable							
B	RW	COUNTER			Counter enable for watchdog and wake-up timer							
			DISABLE	0	Disable							
			ENABLE	1	Enable							
C	RW	LS			Clock levelshifter enable for watchdog and wake-up timer							
			DISABLE	0	Disable							
			ENABLE	1	Enable							

9.4.45 WDPWRUPSTROBE

Address offset: 0x5F

Strobe for register WDPWRUPVALUE

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	W	STROBE			Strobe for register WDPWRUPVALUE							
			NOEFFECT	0	No effect							
			STROBE	1	Strobe							

9.4.46 WDKICK

Address offset: 0x60

Watchdog kick

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	W	KICK			Watchdog counter reset							
			NOEFFECT	0	No effect							
			KICK	1	Reset counter							

9.4.47 WDREQPOWERDOWN

Address offset: 0x62

Enter hibernate mode

Bit number					7	6	5	4	3	2	1	0
ID											B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	HARDPOWERDOWN			Enter hibernate mode							
			NOREQUEST	0	No effect							
			REQUEST	1	Enter hibernate mode							
B	RW	RESERVED0			Reserved0. Do not write '1' to bits marked as RESERVEDn.							

9.4.48 GPIOOUTSET

Address offset: 0x69

GPIO output value SET

Bit number						7	6	5	4	3	2	1	0
ID											C	B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW W1S	GPIO0OUTSET			Set GPIO0								
			NOEFFECT	0	No effect								
			SET	1	Set output high								
B	RW W1S	GPIO1OUTSET			Set GPIO1								
			NOEFFECT	0	No effect								
			SET	1	Set output high								
C	RW W1S	GPIO2OUTSET			Set GPIO2								
			NOEFFECT	0	No effect								
			SET	1	Set output high								

9.4.49 GPIOOUTCLR

Address offset: 0x6A

GPIO output value CLEAR

Bit number						7	6	5	4	3	2	1	0
ID											C	B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW W1C	GPIO0OUTCLR			Clear GPIO0								
			NOEFFECT	0	No effect								
			CLR	1	Set output low								
B	RW W1C	GPIO1OUTCLR			Clear GPIO1								
			NOEFFECT	0	No effect								
			CLR	1	Set output low								
C	RW W1C	GPIO2OUTCLR			Clear GPIO2								
			NOEFFECT	0	No effect								
			CLR	1	Set output low								

9.4.50 GPIOIN

Address offset: 0x6B

GPIO input value

Bit number					7	6	5	4	3	2	1	0
ID										C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	R	GPIO0IN			GPIO0 input value							
			LOW	0	Input is low							
			HIGH	1	Input is high							
B	R	GPIO1IN			GPIO1 input value							
			LOW	0	Input is low							
			HIGH	1	Input is high							
C	R	GPIO2IN			GPIO2 input value							
			LOW	0	Input is low							
			HIGH	1	Input is high							

9.4.51 GPIO0CONF

Address offset: 0x6C

GPIO0 configuration

Bit number					7	6	5	4	3	2	1	0
ID					F	E	D			C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	DIRECTION			Direction							
			INPUT	0	Input							
			OUTPUT	1	Output							
B	RW	INPUT			Input buffer							
			DISABLED	0	Input disabled. Input value is 0.							
			ENABLED	1	Input enabled							
C	RW	PULLDOWN			Pulldown							
			DISABLED	0	Disabled							
			ENABLED	1	Enabled							
D	RW	DRIVE			Drive strength							
			NORMAL	0	Normal drive strength							
			HIGH	1	High drive strength							
E	RW	SENSE			Input type							
			SCHMITT	0	Schmitt trigger input							
			CMOS	1	CMOS input							
F	RW	RESERVED0			Reserved0. Do not write '1' to bits marked as RESERVEDn.							

9.4.52 GPIO1CONF

Address offset: 0x6D

GPIO1 configuration

Bit number					7	6	5	4	3	2	1	0
ID					F	E	D			C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	DIRECTION			Direction							
			INPUT	0	Input							
			OUTPUT	1	Output							

Bit number					7	6	5	4	3	2	1	0
ID					F	E	D			C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
B	RW	INPUT			Input buffer							
			DISABLED	0	Input disabled. Input data is 0.							
			ENABLED	1	Input enabled							
C	RW	PULLDOWN			Pulldown							
			DISABLED	0	Disabled							
			ENABLED	1	Enabled							
D	RW	DRIVE			Drive strength							
			NORMAL	0	Normal drive strength							
			HIGH	1	High drive strength							
E	RW	SENSE			Input type							
			SCHMITT	0	Schmitt trigger input							
			CMOS	1	CMOS input							
F	RW	RESERVED0			Reserved0. Do not write '1' to bits marked as RESERVEDn.							

9.4.53 GPIO2CONF

Address offset: 0x6E

GPIO2 configuration

Bit number					7	6	5	4	3	2	1	0
ID					F	E	D			C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	DIRECTION			Direction							
			INPUT	0	Input							
			OUTPUT	1	Output							
B	RW	INPUT			Input buffer							
			DISABLED	0	Input disabled. Input data is 0.							
			ENABLED	1	Input enabled							
C	RW	PULLDOWN			Pulldown							
			DISABLED	0	Disabled							
			ENABLED	1	Enabled							
D	RW	DRIVE			Drive strength							
			NORMAL	0	Normal drive strength							
			HIGH	1	High drive strength							
E	RW	SENSE			Input type							
			SCHMITT	0	Schmitt trigger input							
			CMOS	1	CMOS input							
F	RW	RESERVED0			Reserved0. Do not write '1' to bits marked as RESERVEDn.							

9.4.54 LDO0CTRL

Address offset: 0x71

LDO0 current limiter, output high-impedance and pulldown control

Bit number						7	6	5	4	3	2	1	0
ID								E	D	C	B	A	A
Reset 0x10						**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	ILIMITVALUE			Current limiter level								
			50MA	0	50 mA								
			100MA	1	100 mA								
			150MA	2	150 mA								
			UNLIMITED	3	Unlimited								
B	RW	HIGHZ			Output high impedance								
			DISABLED	0	Disabled								
			ENABLED	1	Enabled								
C	RW	PULLDOWN			Output pulldown								
			DISABLED	0	Disabled								
			ENABLED	1	Enabled								
D	RW	ENAILIMITAFTERSTAR			Current limiter after LDO start								
			OFF	0	Off								
			ON	1	On								
E	RW	ENAILIMITDURINGSTART			Current limiter during LDO start								
			OFF	0	Off								
			ON	1	On								

9.4.55 LDO1CTRL

Address offset: 0x73

LDO1 current limiter, output high-impedance and pulldown control

Bit number						7	6	5	4	3	2	1	0
ID							G	F	E	D	C	B	A
Reset 0x10						**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	ILIMITVALUE			Current limiter level								
			150MA	0	150mA								
			UNLIMITED	1	Unlimited								
B	RW	RESERVED0			Reserved0. Do not write '1' to bits marked as RESERVEDn.								
C	RW	HIGHZ			Output high impedance								
			DISABLED	0	Disabled								
			ENABLED	1	Enabled								
D	RW	PULLDOWN			Output pulldown								
			DISABLED	0	Disabled								
			ENABLED	1	Enabled								
E	RW	ENAILIMITAFTERSTART			Current limiter after LDO start								
			OFF	0	Off								
			ON	1	On								
F	RW	ENAILIMITDURINGST			Current limiter during LDO start								
			OFF	0	Off								
			ON	1	On								
G	RW	RESERVED1			Reserved1. Do not write '1' to bits marked as RESERVEDn.								

9.4.56 OVERRIDEPWRUPBUCK

Address offset: 0xAB

Override for disabling BUCK1 or/and BUCK2 regulators

Bit number					7	6	5	4	3	2	1	0
ID					H	G	F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	RESERVED0			Reserved0. Do not write '1' to bits marked as RESERVEDn.							
B	RW	BUCK1PWRUPOVERF			BUCK1 power up override							
			DISABLED	0	Disabled							
			ENABLED	1	Enabled							
C	RW	BUCK2PWRUPOVERRIDE			BUCK2 power up override							
			DISABLED	0	Disabled							
			ENABLED	1	Enabled							
D	RW	SPARE0			Spare0							
E	RW	RESERVED1			Reserved1.Do not write '1' to bits marked as RESERVEDn.							
F	RW	BUCK1PWRUPOVERF			BUCK1 power up override setting							
			DISABLED	0	Disable BUCK1							
			NOEFFECT	1	No effect							
G	RW	BUCK2PWRUPOVERRIDEVALUE			BUCK2 power up override setting							
			DISABLED	0	Disable BUCK2							
			NOEFFECT	1	No effect							
H	RW	SPARE1			Spare1							

10 Ordering information

This chapter contains information on IC marking, ordering codes, and container sizes.

10.1 IC marking

The nPM6001 PMIC package is marked as shown in the following figure.

N	P	M	6	0	0	1
<P	P>	<V	V>	<H>	<P>	<F>
<Y	Y>	<W	W>	<L	L>	

Figure 33: IC marking

10.2 Box labels

The following figures define the box labels used for the nPM6001.

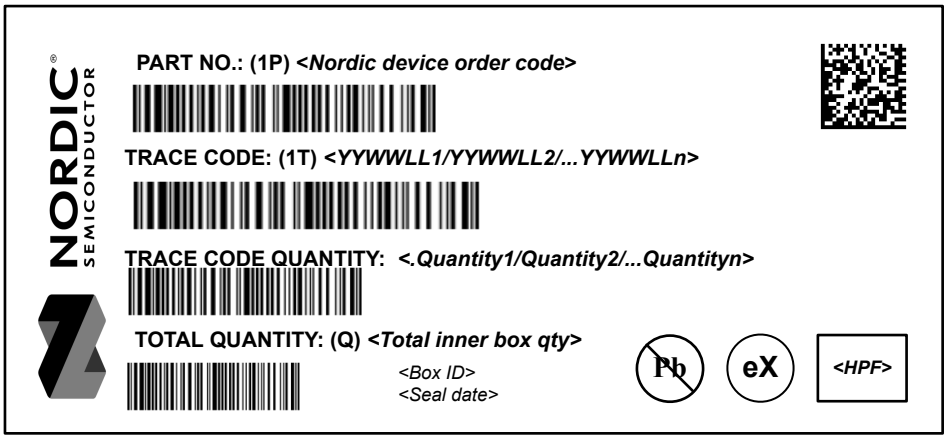


Figure 34: Inner box label

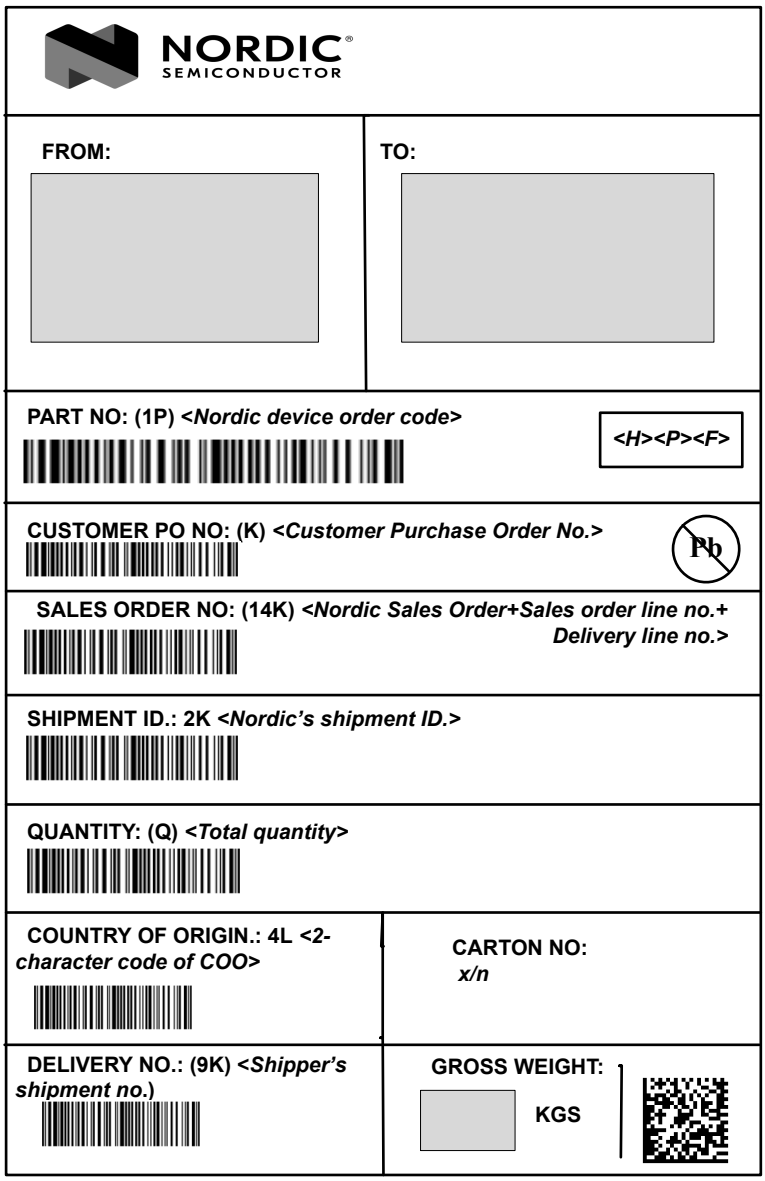


Figure 35: Outer box label

10.3 Order code

The following tables define the nPM6001 order codes and definitions.

n	P	M	6	0	0	1	-	<P	P>	<V	V>	-	<C	C>

Figure 36: Order code

Abbreviation	Definition and implemented codes
N60/nPM60	nPM60 series product
01	Part code
<PP>	Package variant code
<VV>	Function variant code
<H><P><F>	Build code H - Hardware version code P - Production configuration code (production site, etc.) F - Firmware version code (only visible on shipping container label)
<YY><WW><LL>	Tracking code YY - Year code WW - Assembly week number LL - Wafer lot code
<CC>	Container code
eX	2nd Level Interconnect Symbol where value of X is based on J-STD-609

Table 32: Abbreviations

10.4 Code ranges and values

The following tables define the nPM6001 code ranges and values.

<PP>	Package	Size (mm)	Pin/Ball count	Pitch (mm)
CA	WLCSP	2.175x3.635 mm	45	

Table 33: Package variant codes

<VV>	Flash (kB)	RAM (kB)
AA	n/a	n/a

Table 34: Function variant codes

<H>	Description
[A . . Z]	Hardware version/revision identifier (incremental)

Table 35: Hardware version codes

<P>	Description
[0 . . 9]	Production device identifier (incremental)
[A . . Z]	Engineering device identifier (incremental)

Table 36: Production configuration codes

<F>	Description
[A . . N, P . . Z]	Version of preprogrammed firmware
[0]	Delivered without preprogrammed firmware

Table 37: Production version codes

<YY>	Description
[16 . . 99]	Production year: 2016 to 2099

Table 38: Year codes

<WW>	Description
[1 . . 52]	Week of production

Table 39: Week codes

<LL>	Description
[AA . . ZZ]	Wafer production lot identifier

Table 40: Lot codes

<CC>	Description
R7	7" Reel
R	13" Reel

Table 41: Container codes

10.5 Product options

The following tables define the nPM6001 product options.

Order code	MOQ[1]	Comment
nPM6001-CAAA-R	7000	
nPM6001-CAAA-R7	1500	

Table 42: nPM6001 order codes

Order code	Description
nPM6001-EK	Evaluation kit

Table 43: Development tools order code

[1] Minimum Ordering Quantity

11 Legal notices

By using this documentation you agree to our terms and conditions of use. Nordic Semiconductor may change these terms and conditions at any time without notice.

Liability disclaimer

Nordic Semiconductor ASA reserves the right to make changes without further notice to the product to improve reliability, function, or design. Nordic Semiconductor ASA does not assume any liability arising out of the application or use of any product or circuits described herein.

Nordic Semiconductor ASA does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. If there are any discrepancies, ambiguities or conflicts in Nordic Semiconductor's documentation, the Product Specification prevails.

Nordic Semiconductor ASA reserves the right to make corrections, enhancements, and other changes to this document without notice.

Customer represents that, with respect to its applications, it has all the necessary expertise to create and implement safeguards that anticipate dangerous consequences of failures, monitor failures and their consequences, and lessen the likelihood of failures that might cause harm, and to take appropriate remedial actions.

Nordic Semiconductor ASA assumes no liability for applications assistance or the design of customers' products. Customers are solely responsible for the design, validation, and testing of its applications as well as for compliance with all legal, regulatory, and safety-related requirements concerning its applications.

Nordic Semiconductor ASA's products are not designed for use in life-critical medical equipment, support appliances, devices, or systems where malfunction of Nordic Semiconductor ASA's products can reasonably be expected to result in personal injury. Customer may not use any Nordic Semiconductor ASA's products in life-critical medical equipment unless adequate design and operating safeguards by customer's authorized officers have been made. Customer agrees that prior to using or distributing any life-critical medical equipment that include Nordic Semiconductor ASA's products, customer will thoroughly test such systems and the functionality of such products as used in such systems.

Customer will fully indemnify Nordic Semiconductor ASA and its representatives against any damages, costs, losses, and/or liabilities arising out of customer's non-compliance with this section.

RoHS and REACH statement

Refer to www.nordicsemi.com for complete hazardous substance reports, material composition reports, and latest version of Nordic's RoHS and REACH statements.

Trademarks

All trademarks, service marks, trade names, product names, and logos appearing in this documentation are the property of their respective owners.

Copyright notice


QUALITY SYSTEM CERTIFICATION
DNV
ISO 9001