nPM1300

Objective Product Specification

v0.7

NORDIC® SEMICONDUCTOR

nPM1300

nPM1300 is a highly integrated Power Management IC (PMIC) for rechargeable applications. It has several power and system management features which can be implemented with dedicated components. Flexible power regulation and a linear-mode lithium-ion (Li-ion), lithium-polymer (Li-poly), and lithium iron phosphate ($LiFePO_4$) battery charger offer power management in a compact 3.1x2.4 mm WLCSP or 5x5 mm QFN32 package with a minimum of 5 passive components for operation.

nPM1300 supports charging up to 800 mA and delivers up to 600 mA of adjustable regulated voltage. Power can be supplied from two configurable, dual mode 200 mA BUCK regulators and two dual purpose 50 mA LDO/load switches to external components.

The host can read battery temperature, voltage, and current, which are utilized by a fuel gauge algorithm in the nRF Connect Software Development Kit. The fuel gauge provides the battery with state-of-charge estimates comparable to Coulomb counters at a significantly lower power consumption.

Low quiescent current (IQ) extends battery life during shipping and storage with Ship mode. This is also achievable during operation with auto-controlled Hysteretic mode for high efficiency down to 1 µA loads.

The integrated system management features reduce the cost and size of applications. The following integrated features are found in the device:

- System-level watchdog
- Intelligent power-loss warning
- Ship and Hibernate modes for increased battery life
- 5 GPIOs and 3 LED drivers
- Fuel gauge when paired with a nRF52 or 53 Series host device

System management features and I/Os are configured through TWI — I^2C compatible two-wire Interface (TWI).

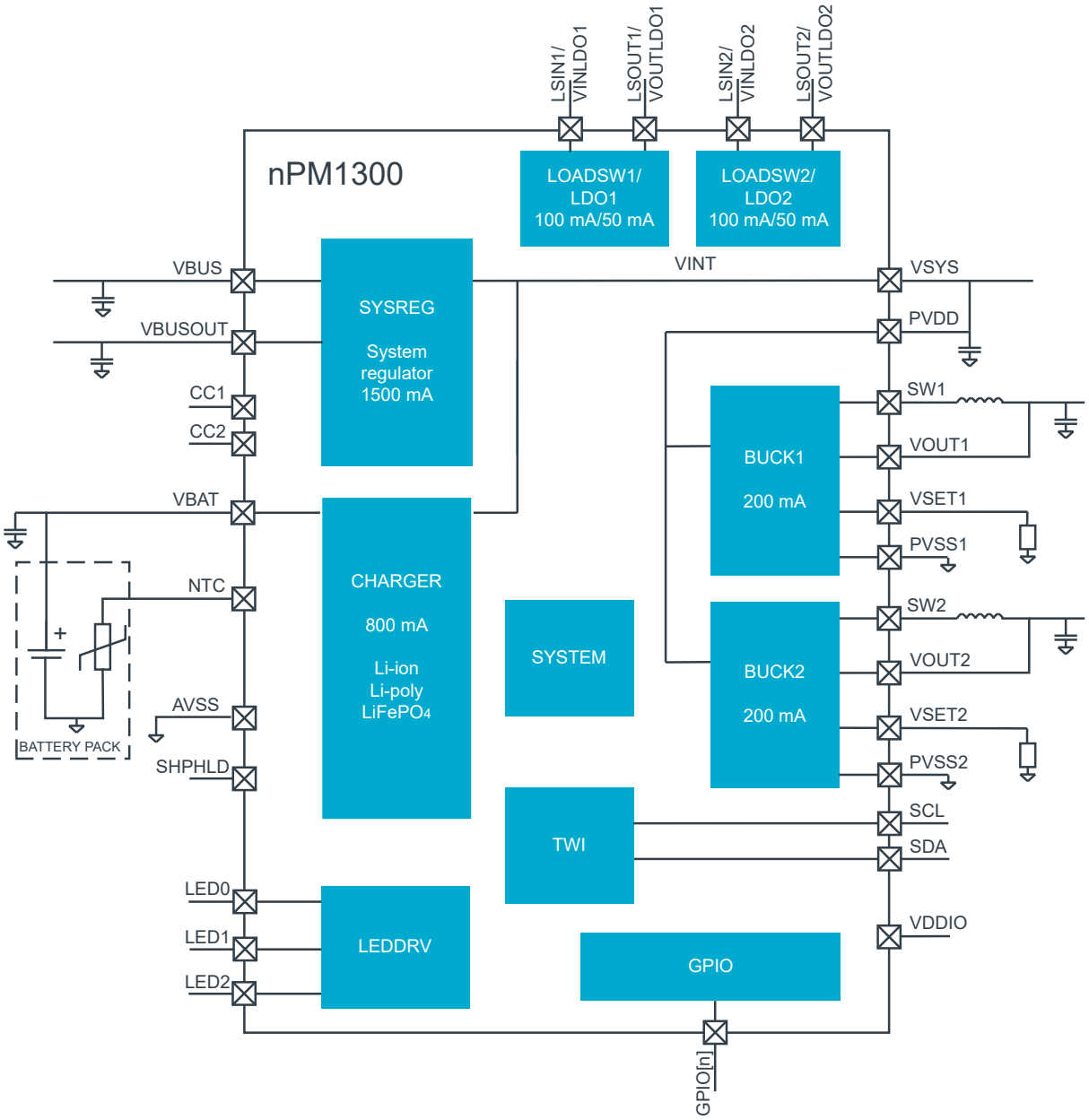

Figure 1: nPM1300

Key features

Features:

- 800 mA linear battery charger
  - Linear charger for lithium-ion, lithium-polymer, and lithium iron phosphate batteries
  - Adjustable charge current up to 800 mA
  - Adjustable thermal regulation
  - User selectable charging termination voltage between 3.5 V and 4.45 V
  - JEITA compliant
  - Dynamic power-path management
- Input current limiter
  - USB Type-C compliant
  - 4.0 V to 5.5 V input voltage range
  - 22 V tolerant
- Two 200 mA buck regulators
  - Automatic transition between hysteretic and pulse width modulation (PWM) modes
  - Forced PWM mode for clean power operation
  - Pin-selectable output voltage
- Two 50mA LDO/100 mA load switches
- 10-bit ADC for system monitoring
  - Measures VBUS voltage, battery voltage, current, and die temperature
- Three LED drivers with 5 mA low-side that run automatically or are software controlled
- Watchdog timer with selectable reset or power cycling
- Power-fail warning (POF)
- Failed boot timer
- Long press hard reset
- General purpose GPIOs that can control BUCKs, load switches, interrupt output, reset, power fail warning, or as a general purpose I/O
- Package options available:
  - 3.1x2.4 mm WLCSP package
  - 5.0x5.0 mm QFN package

Applications:

- Wearables
  - Health/fitness sensor and monitor devices
- Computer peripherals and I/O devices
  - Mouse
  - Keyboard
  - Multi-touch trackpad
- Asset trackers
- Interactive entertainment devices
  - Remote controls
  - Gaming controllers
- IoT applications
  - Smart/low-energy sensors
  - Loggers
  - Actuator controls

Contents

1 Revision history

Date	Version	Description
June 2023	0.7	Preliminary release

2 About this document

This document is organized into chapters that are based on the modules available in the IC.

2.1 Document status

The document status reflects the level of maturity of the document.

Document name	Description
Objective Product Specification (OPS)	Applies to document versions up to 1.0. This document contains target specifications for product development.
Product Specification (PS)	Applies to document versions 1.0 and higher. This document contains final product specifications. Nordic Semiconductor ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Table 1: Defined document names

2.2 Core component chapters

Every core component has a unique capitalized name or an abbreviation of its name, e.g. LED, used for identification and reference. This name is used in chapter headings and references, and it will appear in the C-code header file to identify the component.

The core component instance name, which is different from the core component name, is constructed using the core component name followed by a numbered postfix, starting with 0, for example, LED0. A postfix is normally only used if a core component can be instantiated more than once. The core component instance name is also used in the C-code header file to identify the core component instance.

The chapters describing core components may include the following information:

- A detailed functional description of the core component
- Register configuration for the core component
- Electrical specification tables, containing performance data which apply for the operating conditions described in .

2.3 Register tables

Individual registers are described using register tables. These tables are built up of two sections. The first three colored rows describe the position and size of the different fields in the register. The following rows describe the fields in more detail.

2.3.1 Fields and values

The **Id (Field Id)** row specifies the bits that belong to the different fields in the register. If a field has enumerated values, then every value will be identified with a unique value id in the **Value Id** column.

A blank space means that the field is reserved and read as undefined, and it also must be written as `0` to secure forward compatibility. If a register is divided into more than one field, a unique field name is specified for each field in the **Field** column. The **Value Id** may be omitted in the single-bit bit fields when values can be substituted with a Boolean type enumerator range, e.g. true/false, disable(d)/enable(d), on/off, and so on.

Values are usually provided as decimal or hexadecimal. Hexadecimal values have a `0x` prefix, decimal values have no prefix.

The **Value** column can be populated in the following ways:

- Individual enumerated values, for example 1, 3, 9.
- Range of values, e.g. [0..4], indicating all values from and including 0 and 4.
- Implicit values. If no values are indicated in the **Value** column, all bit combinations are supported, or alternatively the field's translation and limitations are described in the text instead.

If two or more fields are closely related, the **Value Id**, **Value**, and **Description** may be omitted for all but the first field. Subsequent fields will indicate inheritance with '..'.

A feature marked **Deprecated** should not be used for new designs.

2.3.2 Permissions

Different fields in a register might have different access permissions enforced by hardware.

The access permission for each register field is documented in the **Access** column in the following ways:

Access	Description	Hardware behavior
RO	Read-only	Field can only be read. A write will be ignored.
WO	Write-only	Field can only be written. A read will return an undefined value.
RW	Read-write	Field can be read and written multiple times.
W1	Write-once	Field can only be written once per reset. Any subsequent write will be ignored. A read will return an undefined value.
RW1	Read-write-once	Field can be read multiple times, but only written once per reset. Any subsequent write will be ignored.

Table 2: Register field permission schemes

3 Product overview

This chapter contains an overview of the main features found in nPM1300.

3.1 Block diagram

The block diagram illustrates the overall system.

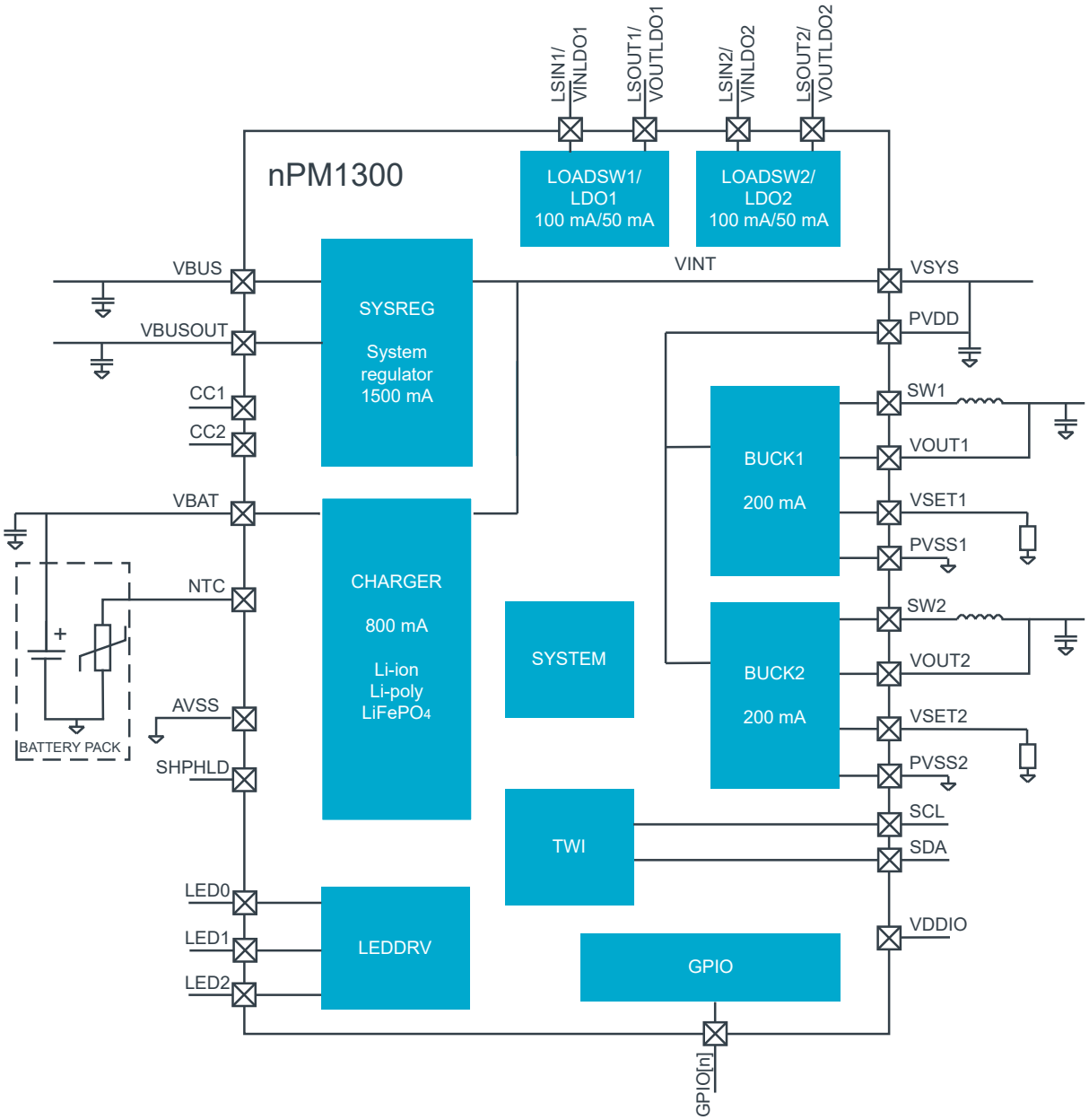

Figure 2: Block diagram

3.1.1 In-circuit configurations

The device is configurable for different applications and battery characteristics through input pins.

The following pins must be configured before power-on reset. For the full pin list, see Pin assignments on page 127.

Pin	Function	Reference
VDDIO	Supply for the TWI control interface and GPIOs	Interface supply on page 98, GPIO — General purpose input/output on page 62
VSET1	BUCK1 enable and VOUT1 voltage level selection at power-on reset	BUCK — Buck regulators on page 41
VSET2	BUCK2 enable and VOUT2 voltage level selection at power-on reset	BUCK — Buck regulators on page 41
CC1, **CC2**	USB charger detection (USB Type-C)	USB port detection on page 18

Table 3: In-circuit configurations

3.2 System description

The device has the following core components that are described in detail in their respective chapters.

- SYSREG — System regulator on page 18
- CHARGER — Battery charger on page 23
- BUCK — Buck regulators on page 41
- LOADSW/LDO — Load switches/LDO regulators on page 54
- LEDDRV — LED drivers on page 59
- GPIO — General purpose input/output on page 62

The system regulator (SYSREG) is supplied by VBUS. It supports 4.0 V to 5.5 V for internal functions and tolerates transient voltages up to 22 V. Overvoltage protection is implemented for both internal and external circuitry. SYSREG also implements current limiting for VBUS to comply with the USB Type-C specification. SYSREG supports Type-C charger detection.

The battery charger (CHARGER) is a JEITA compliant linear battery charger for lithium-ion (Li-ion), lithium-polymer (Li-poly), and lithium iron phosphate ($LiFePO_4$) batteries. CHARGER controls the charge cycle using a standard Li-ion charge profile. CHARGER implements dynamic power-path management regulating current in and out of the battery, depending on system requirements, to ensure immediate system operation if the battery is depleted. Safety features, such as battery temperature monitoring and charger thermal regulation are supported.

Two highly efficient buck regulators (BUCK) supply the application circuitry and offer several output voltage options. BUCK is controlled through registers or GPIO pins. Default output voltage can be set with external resistors.

Input for the two load switches (LOADSW/LDO) can function as switches or linear voltage regulators to complement the power distribution network. LOADSW is controlled through registers or GPIO pins.

The system monitor provides measurements such as battery voltage, battery current, VBUS, battery and die temperatures.

General purpose input/output pins (GPIO) are configurable as charge state and warning indicators, on-chip power supply, and load switch control.

The device also features Ship and Hibernate modes, the lowest quiescent current states. They disconnect the battery from the system and reduce the quiescent current of the device to extend battery life. Hibernate mode can be utilized during normal operation as the device can autonomously wake-up after a preconfigured timeout. This makes it possible to extend battery life to the maximum capacity.

3.3 Power-on reset (POR) and brownout reset (BOR)

The device is supplied by **VBUS** or **VBAT**.

When one of the following conditions are met, a power-on reset (POR) occurs.

- **VBUS** > $VBUS_{POR}$
- **VBAT** > $VBAT_{POR}$

When both of the following conditions are met, a brownout reset (BOR) occurs.

- **VBUS** < $VBUS_{BOR}$
- **VBAT** < $VBAT_{BOR}$

3.4 Supported battery types

The charger supports rechargeable Li-ion, Li-polymer, or $LiFePO_4$ batteries.

Battery packs connected to the **VBAT** pin must contain the following protection circuitry:

- Overvoltage protection
- Undervoltage protection
- Overcurrent discharge protection
- Thermal fuse to protect from overtemperature (if NTC thermistor is not present)

3.5 Thermal protection

A global thermal shutdown is triggered when the die temperature exceeds the operating temperature range, see TSD. All device functions are disabled in thermal shutdown. The device functions are re-enabled when the temperature is sufficiently reduced according to a hysteresis TSD_{HYST}.

A secondary mechanism exists that will disable the charger when the die reaches the host software programmable temperature of DIETEMPSTOP on page 38 . Once this temperature is reached, the charging will stop but all other functionality will remain active. Charging will restart when the die temperature reduces to the host software programmable temperature of DIETEMPRESUME on page 38

3.6 System electrical specification

Symbol	Description	Min.	Typ.	Max.	Unit
IQ_{SHIP}	Ship mode quiescent current		370		nA
IQ_{SHIPT}	Hibernate mode quiescent current		500		nA
IQ_{BAT}	Quiescent current, battery operation, no load, VBUS disconnected		TBD		nA
TSD	Thermal shutdown threshold		120		°C
TSD_{HYST}	Thermal shutdown hysteresis		10		°C

Table 4: System electrical specification

3.7 System efficiency

Described here is the characterization of the power path from the battery supply (**VBAT**) to the BUCK output (**VOUT**) under different battery voltages, output voltages, and load current conditions.

In the following figure, the load current is swept from 1 µA to 200 mA and back to capture mode change hysteresis.

4 Absolute maximum ratings

Maximum ratings are the extreme limits to which the device can be exposed for a limited amount of time without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the device.

Pin	Note	Min.	Max.	Unit
VBUS	Power	-0.3	22	V
VBAT, **VSYS**, **VBUSOUT**, **PVDD**	Power	-0.3	5.5	V
AVSS, **PVSS1**, **PVSS2**	Power		0	V
VDDIO	Power	-0.3	5.5	V
NTC, **CC1**, **CC2**, **SHPHLD**, **LED0**, **LED1**, **LED2**, **LSIN1/VINLDO1**, **LSOUT1/VOUTLDO1**, **LSIN2/VINLDO2**, **LSOUT2/VOUTLDO2**, **VSET1**, **VSET2**, **VOUT1**, **VOUT2**, **SW1**, **SW2**	Analog pins	-0.3	VSYS+0.3	V
GPIO[0..4], **SDA**, **SCL**	Digital pins	-0.3	VDDIO+0.3	V

Table 5: Absolute maximum ratings

	Note	Min.	Max.	Unit
Storage temperature		-40	+125	°C
MSL QFN	Moisture sensitivity level		2	
MSL WLCSP	Moisture sensitivity level		1	
ESD HBM	Human Body Model Class 2		2	kV
ESD CDM	Charged Device Model		500	V

Table 6: Environmental ratings (WLCSP)

5 Recommended operating conditions

The operating conditions are the physical parameters that the chip can operate within.

Symbol	Description	Min.	Max	Unit
$VBUS_{OP}$	Supply voltage	4.0	5.5	V
$VBAT_{OP}$	Battery voltage	2.3	4.45	V
VDDIO	I/O supply voltage	1.7	VSYS	V
T_J	Junction temperature	-40	+125	°C
T_A	Ambient temperature	-40	+85	°C

Table 7: Recommended operating conditions

5.1 Dissipation ratings

Thermal resistances and thermal characterization parameters as defined by JESD51-7 are shown in the following tables.

Symbol	Parameter	QFN 32 pins	Units
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	24.24	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	10.71	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	8.84	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.15	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	8.90	°C/W

Table 8: Thermal resistances and characterization parameters, QFN32

Symbol	Parameter	WLCSP 35 pins	Units
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	48.34	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	6.02	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	22.99	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.53	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	23.38	°C/W

Table 9: Thermal resistances and characterization parameters, WLCSP

5.2 WLCSP light sensitivity

WLCSP package is sensitive to light.

All WLCSP package variants are sensitive to visible and close-range infrared light. The final product design must shield the chip through encapsulation or shielding/coating the WLCSP device.

WLCSP package variant CAAA has a backside coating that covers the marking side of the device with a light absorbing film. The side edges and the ball side of the device are still exposed and need to be protected.

6 Core Components

6.1 SYSREG — System regulator

6.1.1 VBUS input current limiter

The VBUS input current limiter manages VBUS current limitation and charger detection for USB Type-C compatible chargers.

It supplies the VINT node but does not regulate its voltage. VBUS is seen at VSYS as a supply, provided that VBUS is within specified limits.

There are two USB compliant, accurate current limits: $IBUS_{100MA}$ (100 mA) and $IBUS_{500MA}$ (500 mA).

In addition, there are current limits in 100 mA steps from 600 mA to 1500 mA. The 1500 mA limit is compatible with USB Type-C.

The default current limit is $IBUS_{100MA}$ (100 mA).Host software can configure the current in register VBUSINILIM0 on page 21

6.1.2 VBUS overvoltage protection

The overvoltage threshold for **VBUS** is $VBUS_{OVP}$. The undervoltage threshold for **VBUS** is $VBUS_{MIN}$.

SYSREG is disabled when $VBUS_{voltage}$ is above the overvoltage threshold $VBUS_{OVP}$, or below the undervoltage threshold $VBUS_{MIN}$. This isolates **VBUS** and prevents current flowing from VINT to **VBUS**.

6.1.3 USB port detection

USB charger detection is on pins **CC1** and **CC2**. These pins must be connected directly to the USB connector for detection to happen.

These pins have internal pull-downs with resistance equal to R_d.

When the device is plugged into a wall adaptor or USB power source, USB port detection runs automatically. One of the CC lines is connected to a pull-up at the source. The other CC line stays pulled down. The voltage over the corresponding R_d determines if a connection was made and if SYSREG can deliver 500 mA or higher current.

Comparators with thresholds at V_{RDCONN}, V_{RD1A5}, and V_{RD3A} monitor CC line voltage when VBUS is present. All comparator output is debounced with t_{RDDEB} and available to host software through register USBCDETECTSTATUS on page 22.

If enabled, an interrupt is issued to the host whenever a threshold is crossed (when voltage decreases or increases). The events are visible in register EVENTSVBUSIN1SET on page 116.

The USB power source capability is detected by one of the CCs at a time, depending on the orientation of the USB plug on the device. The other CC line remains at 0 V. The charger type is defined in the VBUSINCC1CMP or VBUSINCC2CMP field, depending on which pin is used for connection.

The default VBUS current limit of 100 mA is used until a CC is detected. Host software can update the VBUS current limit in VBUSINILIM0 on page 21 after device detection. When a USB cable is unplugged and plugged back in, or a reset occurs, the default current limit VBUSIN.ILIM.STARTUP is used.

When TASKUPDATEILIMSW is written, the default current limit is used when the following occur:

- A reset

- The USB cable is unplugged and plugged back in

If USB Type-C configuration is not used, **CC1** and **CC2** can be left floating or connected to ground. The default VBUS current limit will remain at 100 mA until the host negotiates and configures a higher current.

Note: When VBUS is removed, EVENT.VBUS.UNDVOLT.DETECTED is set first followed by EVENT.VBUS.REMOVED and EVENT.VBUS.OVRVOLT.DETECTED. When VBUS is applied, EVENT.VBUS.DETECTED is set followed by EVENT.VBUS.UNDVOLT.REMOVED and EVENT.VBUS.OVRVOLT.REMOVED, depending on the VBUS voltage.

6.1.4 USB2.0 suspend mode

The device cannot detect suspend mode, but must be informed by host software through the TWI (register VBUSSUSPEND on page 21) to minimize current consumption from VBUS to I_{SUSP}.

The current consumed through pin **VBUSOUT** is not included. VBUS is then disconnected from VSYS but VBUSOUT remains active. As a consequence, charging is paused. The device exits this mode only when instructed by the host software through a TWI command. Charging resumes automatically.

6.1.5 Electrical specification

Symbol	Description	Min.	Typ.	Max.	Unit
$VBUS_{MIN}$	Under-voltage threshold		3.6		V
$VBUS_{OVP}$	Overvoltage protection threshold		5.5		V
$VBUS_{POR}$	Power-on reset release voltage for VBUS		3.9		V
$VBUS_{BOR}$	Brown-out reset trigger for VBUS		3.8		V
$IBUS_{100MA}$	VBUS input current limit, 100 mA [1]			95	mA
$IBUS_{500MA}$	VBUS input current limit, 500 mA [1]			495	mA
$IBUS_{LIMACC}$	Accuracy of IBUS current limit (steps from 600 to 1500 mA)[1]	-10		+10	%
I_{SUSP}	VBUS current consumption in suspend mode. Current from VBUSOUT is excluded.		1.8		mA
Ron	Resistance between VBUS and VSYS (VBUSINLIM0=15 (1.5 A), VBUS=5 V)		300		mOhm
$R_{VBUSOUT}$	On-resistance of the VBUSOUT switch (VBUS=5.0 V)		10		Ohm
R_d	Pull-down resistance on pins CC1 and CC2		5.1		kOhm
V_{RDCONN}	Threshold to detect connection		0.2		V
V_{RD1A5}	Threshold to detect charger type on CC1 or CC2 pins		0.66		V
V_{RD3A}	Threshold for 3 A current limit		1.23		V
t_{RDDEB}	Debounce time for CC voltage level detection		15		ms

Table 10: VBUSIN electrical specification

[1] Includes internal device consumption and current flowing through pin **VBUSOUT**.

6.1.6 Electrical characteristics

The following graphs show VBUSIN's electrical characteristics.

6.1.7 Registers

Instances

Instance	Base address	Description
VBUSIN	0x00000200	VBUSIN Registers VBUSIN register map

Register overview

Register	Offset	Description
TASKUPDATEILIMSW	0x0	Select Input Current limit for VBUS

Register	Offset	Description
VBUSINILIM0	0x1	Select Input Current limit for VBUS NOTE: Reset value from OTP, value listed in this table may not be correct.
VBUSSUSPEND	0x3	Suspend mode enable
USBCDETECTSTATUS	0x5	VBUS CC comparator status flags
VBUSINSTATUS	0x7	VBUS status flags

6.1.7.1 TASKUPDATEILIMSW

Address offset: 0x0

Select Input Current limit for VBUS

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKUPDATEILIM			Set to switch from vbusinIlimStartup to vbusinIlim0								
			NOEFFECT	0	No effect								
			SELVBUSILIM0	1	Set to use vbusinilim0. Vbus removal results in switch back to vbusinIlimStartup								

6.1.7.2 VBUSINILIM0

Address offset: 0x1

Select Input Current limit for VBUS NOTE: Reset value from OTP, value listed in this table may not be correct.

Bit number						7	6	5	4	3	2	1	0
ID										A	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	VBUSINILIM0			Input current limit for VBUS selected by Host								
			500MA0	0	500mA								
			100MA	1	100mA								
			NOTUSED2	2	100mA (reserved)								
			NOTUSED3	3	100mA (reserved)								
			NOTUSED4	4	100mA (reserved)								
			500MA	5	500mA								
			600MA	6	600mA								
			700MA	7	700mA								
			800MA	8	800mA								
			900MA	9	900mA								
			1000MA	10	1000mA								
			1100MA	11	1100mA								
			1200MA	12	1200mA								
			1300MA	13	1300mA								
			1400MA	14	1400mA								
			1500MA	15	1500mA								

6.1.7.3 VBUSSUSPEND

Address offset: 0x3

Suspend mode enable

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	VBUSSUSPENDENA			VBUS suspend control bit							
			NORMAL	0	Normal mode							
			SUSPENDMODE	1	Suspend Mode							

6.1.7.4 USBCDETECTSTATUS

Address offset: 0x5

VBUS CC comparator status flags

Bit number					7	6	5	4	3	2	1	0
ID										B	A	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	R	VBUSINCC1CMP			CC1 Charger detection comparator output							
			NOCONNECTION	0	no connection							
			DEFAULTUSB	1	Default USB 100/500mA							
			1A5HIGHPOWER	2	1.5A High Power							
			3AHIGHPOWER	3	3A High Power							
B	R	VBUSINCC2CMP			CC2 Charger detection comparator output							
			NOCONNECTION	0	no connection							
			DEFAULTUSB	1	Default USB 100/500mA							
			1A5HIGHPOWER	2	1.5A High Power							
			3AHIGHPOWER	3	3A High Power							

6.1.7.5 VBUSINSTATUS

Address offset: 0x7

VBUS status flags

Bit number					7	6	5	4	3	2	1	0
ID							F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	R	VBUSINPRESENT			Vbus has been detected							
			NOTDETECTED	0	NotDetected							
			DETECTED	1	Detected							
B	R	VBUSINCURRLIMACT			VBUS Current limit detected							
			NOTDETECTED	0	NotDetected							
			DETECTED	1	Detected							
C	R	VBUSINOVRPROTACTIVE			VBUS Over voltage protection Active							
			NOTACTIVE	0	NotActive							
			ACTIVE	1	Active							
D	R	VBUSINUNDERVOLTA			VBUS Under voltage detected							
			NOTDETECTED	0	NotDetected							
			DETECTED	1	Detected							
E	R	VBUSINSUSPENDMODEACTIVE			VBUS suspended							
			NORMAL	0	Normal							
			SUSPEND	1	Suspended							
F	R	VBUSINVBUSOUTACT			VBUS Out is Active							

Bit number															
ID											F	E	D	C	B	A
Reset 0x00									**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description											
			NOTACTIVE	0	NotActive											
			ACTIVE	1	Active											

6.2 CHARGER — Battery charger

The battery charger is suitable for general purpose applications with lithium-ion (Li-ion), lithium-polymer (Li-poly), and lithium iron phosphate ($LiFePO_4$) batteries. The following sections describe how to configure CHARGER to match the battery type.

The main features of the battery charger are the following:

- Linear charger for Li-ion, Li-poly, and $LiFePO_4$ battery chemistries
- Bidirectional power FET for dynamic power-path management
- Automatic trickle, constant current, constant voltage, and end-of-charge/recharge cycle
- JEITA compliant with a configurable battery charging temperature profile

Charging is enabled through host software and the voltage and charging current are configurable. The device manages the charging cycle after the charging parameters are defined.

V_{TERM} must be set to a lower voltage than the battery overvoltage protection.

6.2.1 Charging cycle

Once host software enables charging using register BCHGENABLESET on page 32, battery charging starts after a **VBUS** connection and the battery is detected.

If a battery is detected, trickle charging begins. Constant current charging starts when the battery voltage is above $V_{TRICKLE\_FAST}$. After the battery voltage reaches V_{TERM}, the charger enters constant voltage charging. The battery voltage is maintained while monitoring current flow into the battery. When the current into the battery drops below I_{TERM}, charging is complete. The charger waits until the battery voltage is below $V_{RECHARGE}$ before starting a new charging cycle. Charging is disabled using register BCHGENABLECLR on page 32.

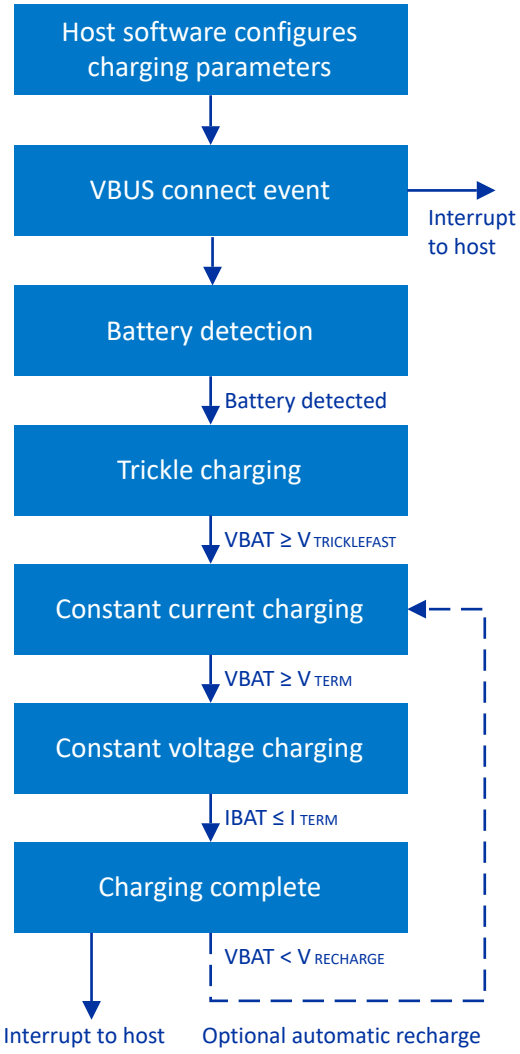

Figure 3: Charging cycle flow chart

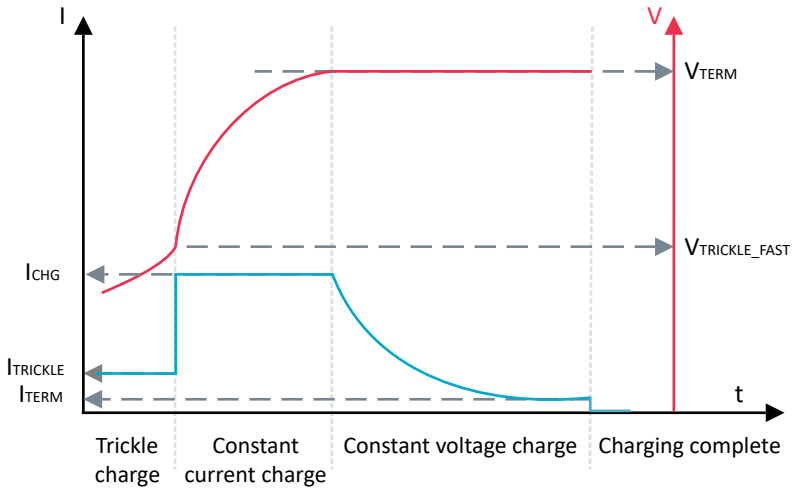

Figure 4: Charging cycle

6.2.2 Battery detection and UVLO

Battery detection and undervoltage lockout (UVLO) release run automatically when charging starts.

UVLO release refers to the overdischarge protection circuit in the battery pack protection circuit. It prevents battery loss when an overdischarge occurs. An undervoltage lockout circuit is not included on the device and must be set up on the battery pack.

CHARGER waits until a battery is detected before charging. If UVLO release fails, then CHARGER retries every 500 ms. A faulty or absent battery is indicated in bit BATTERY.DETECTED, see BCHGCHARGESTATUS on page 39.

If the system resets, charging control bits are reset and charging is disabled by default.

6.2.3 Termination voltage (VTERMSET)

V_{TERM} is configured through TWI according to the battery type in use, see register BCHGVTERM on page 34.

For a higher temperature range, a lower termination voltage, V_{TERMR}, is available and configured separately in register BCHGVTERMR on page 35. V_{TERM} and V_{TERMR} can be set to the same value.

6.2.4 Charge current limit (ICHG)

The charge current limit is set between 32 mA and 800 mA in 2 mA steps. Charging current I_{CHG} is configured with TWI with the default value of 32 mA.

CHARGER must be disabled before changing the current setting in BCHGISETMSB on page 33 and BCHGISETLSB on page 34. The setting takes effect when charging is enabled.

Charge current is configured using a 9-bit value. The decimal code can be calculated as CODE = Current (mA)/2. The following table gives some example charging currents.

I_{CHG}	Code	BCHGISETMSB	BCHGISETLSB
32 mA	16	8	0
34 mA	17	8	1
400 mA	200	100	0
800 mA	400	200	0

Table 11: Charging current

Trickle charging current $I_{TRICKLE}$ is 10% of I_{CHG}. Trickle charging is active when VBAT < $V_{TRICKLE\_FAST}$ (default 2.9 V).

Termination current I_{TERM} is programmable to 10% (default) or 20% of I_{CHG}.

These parameters are configured in registers BCHGVTRICKLESEL on page 35 and BCHGITERMSEL on page 36.

6.2.5 Battery temperature monitoring

CHARGER supports three types of NTC thermistors for battery temperature (T_{BAT}) monitoring. Only one can be enabled at a time.

The host software must select the corresponding setting that matches the battery thermistor before enabling charging in register ADCNTCRSEL on page 81. The following thermistor resistors are supported.

Nominal resistance	Resistance accuracy	B25/50	Beta accuracy	B25/85
10 kΩ	1 %	3380 K	1 %	3434/3435 K
47 kΩ	1 %	4050 K	1 %	4108 K
100 kΩ	1 %	4250 K	1 %	4311 K

Table 12: Supported thermistor resistors

Using these components, a ±2°C accuracy is achievable in the range from 0 °C to 60 °C.

Note: If a capacitor is placed in parallel with the thermistor, the max capacitance is 100 pF.

If a thermistor is not used, the **NTC** pin has to be tied directly to GND or through a resistor. The functionality must be disabled in register BCHGDISABLESET on page 33. This does not impact Charger thermal regulation on page 27 because the two temperature measurements are independent.

The following battery temperature thresholds can be set: $T_{COLD} \leq T_{COOL} \leq T_{WARM} \leq T_{HOT}$. These limits can be set between -20°C and +60°C and it is allowed to set adjacent thresholds to identical values. Setting $T_{WARM} = T_{HOT}$, for example, means that there is no warm region. Charging does not happen below T_{COLD} and above T_{HOT}. Charging can be paused at T_{WARM} rather than T_{HOT} by setting register BCHGCONFIG on page 40.

The thresholds are written into corresponding registers. Codes are calculated using the following equation:

$$code = ROUND\left(2^{10} \cdot \frac{R_T}{R_T + R_B}\right)$$

Figure 5: Equation for battery temperature

R_T is the thermistor resistance at a desired temperature and R_B (internal bias resistor) equals the thermistor resistance at 25°C. See NTCCOLD on page 36, NTCCOOL on page 36, NTCWARM on page 37, and NTCHOT on page 37. Default values in the registers match the JEITA guideline and are intended for the 10 kΩ thermistor defined in the previous table.

Temp.	10 kΩ	47 kΩ	100 kΩ	Register
0°C	749	787	799	NTCCOLD
10°C	658	684	693	NTCCOOL
45°C	337	306	297	NTCWARM
60°C	237	197	186	NTCHOT

Table 13: Battery temperature, example codes

The charging current and termination voltage can be configured for each temperature zone.

Temperature region	Temperature limits, default setting	Charge current	Termination voltage
Cold	$T_{BAT} < T_{COLD} = 0°C$	0 (OFF)	N/A
Cool	$T_{COLD} < T_{BAT} < T_{COOL} = +10°C$	I_{COOL} / I_{CHG} Note	V_{TERM}
Nominal	$T_{COOL} < T_{BAT} < T_{WARM} = +45°C$	I_{CHG}	V_{TERM}
Warm	$T_{WARM} < T_{BAT} < T_{HOT} = +60°C$	I_{CHG}	V_{TERMR}
Hot	$T_{BAT} > T_{HOT}$	0 (OFF)	N/A

Table 14: Battery temperature regions

Note: Default is I_{COOL} (50 % of I_{CHG}) but this lower current setting can be disabled.

Battery temperature is measured by the on-chip ADC at regular intervals during charging. The latest result is available in registers ADCNTCRESULTMSB on page 83 and ADCGP0RESULTLSBS on page 83.

When the battery temperature rises over T_{WARM} or T_{HOT}, or falls below T_{COOL} or T_{COLD}, an interrupt is sent.

6.2.6 Charger thermal regulation

Heat dissipation from the linear charger is managed by setting a maximum temperature limit for the die. This limit must not exceed device and PCB temperature requirements.

Die temperature monitoring is active during charging, with a default limit of $T_{CHGSTOP}$. Charging stops when the die temperature reaches the limit. It resumes when the die cools down to $T_{CHGRESUME}$.

$T_{CHGSTOP}$ controls the junction temperature rise and limits the temperature rise on the PCB and device mechanics. The device can be configured to send an interrupt when the limit is met.

The following equation calculates the temperature limits. T represents the die temperature limit in degrees Celsius.

$$code = ROUND\left(\frac{394.67 - T}{0.7926}\right)$$

Registers DIETEMPSTOP on page 38 and DIETEMPSTOPLSB on page 38 are concatenated to create a 10-bit value that defines the charging stop temperature $T_{CHGSTOP}$. Registers DIETEMPRESUME on page 38 and DIETEMPRESUMELSB on page 38 are concatenated to create a 10-bit value that defines the charging resume temperature $T_{CHGRESUME}$. The host software reads register DIETEMPSTATUS on page 39 to determine if the die temperature is above $T_{CHGSTOP}$.

The following are example codes.

Die temp	50°C	60°C	70°C	80°C	90°C	100°C	110°C
Code (dec.)	435	422	410	397	384	372	359

Table 15: Die temperature, example codes

6.2.7 Charger error conditions

A CHARGER error condition occurs when one of the following are present:

- Trickle charge timeout, see $t_{OUTTRICKLE}$

- Safety timer expires, see $t_{OUTCHARGE}$

After an error is detected, CHARGER is disabled. The charging error indication is activated and the charging indication is deactivated. Error conditions are cleared when **VBUS** is disconnected and reconnected again.

Errors are reported in register BCHGERRREASON on page 40 and BCHGERRSENSOR on page 40.
Host software clears errors with register TASKCLEARCHGERR on page 31 and releases the charger from the error state with TASKRELEASEERR on page 31.

When the safety timer expires, the host must make sure it is safe to charge before resetting TASKCLEARSAFETYTIMER on page 32

6.2.8 Charging status (CHG) and error indication (ERR)

LEDs indicate after bit CHGEN is set when enabling CHARGER.

The LED[n] pins sink 5 mA of current when active. They are high impedance when disabled. This is suitable for driving LEDs or connecting to host GPIOs in a weak pull-up configuration. The LED anode must be connected to a voltage rail that will allow forward bias. If a general purpose open drain output is needed, these LED pins can be used with a pull-up resistor connected to a voltage rail. See LEDDRV — LED drivers on page 59 for further information.

Charging status

Charging status is available in register BCHGCHARGESTATUS on page 39.

LED drivers are configured through TWI to indicate charging is active when in Trickle mode, Constant Current mode, Constant Voltage mode, or charge.

The charging LED turns off when charging is complete. It turns on when charging starts. The charging LED is on when Charger thermal regulation is active (charging is disabled temporarily due to die temp exceeding the configured limit).

The charging status LED is off when battery temperature is below cold or above hot thresholds. No error is indicated in these cases. The charging status LED is off when VBUS > $VBUS_{OVP}$ and no error is indicated.

Error indications

Errors are reported in register BCHGERRREASON on page 40 and BCHGERRSENSOR on page 40.

There is no indication when Charger thermal regulation is active, or when battery temperature is above or below the threshold.

6.2.9 End-of charge and recharge

Charging terminates automatically when the battery voltage reaches V_{TERM} and charging current is less than I_{TERM}. An interrupt is issued to the host.

Unless disabled (bit DISABLE.RECHARGE in BCHGDISABLESET on page 33), charging restarts automatically when VBAT is less than $V_{RECHARGE}$ and an interrupt is sent to the host.

6.2.10 DDPM — Dynamic power-path management

CHARGER manages battery current flow to maintain VSYS voltage.

The system load requirements are prioritized over battery charge current when **VBUS** is connected and the battery is charging. The battery is isolated when **VBUS** is connected and the battery is fully charged. VINT supplies the system load unless the load exceeds the chosen input current limit $IBUS_{LIM}$. When **VBUS** is disconnected, CHARGER supplies the system (VINT) from the battery.

During charging, if the system current load exceeds the current provided by VINT, the battery charge current decreases to maintain VSYS voltage. CHARGER reduces the current to maintain an internal voltage

of $V_{CHDROPOUT}$ above VBAT. If more current is required, CHARGER enters supplement mode to provide current from the battery, up to $IBAT_{LIM}$.

Note: VSYS must not be supplied from an external source.

6.2.11 Discharge current limit

CHARGER current limit is configured through registers BCHGISETDISCHARGEMSB on page 34 and BCHGISETDISCHARGELSB on page 34.

Register BCHGILIMSTATUS on page 39 is read to determine if a current higher than the limit is flowing from VBAT to VSYS. The default value allows a typical current of 1.34 A. The minimum setting is 270 mA. If the system load exceeds $IBAT_{LIM}$, VINT could drop below $VSYS_{POF}$ causing the device to reset, as described in POF — Power-fail comparator on page 85.

The limit is configured using a 9-bit setting according to the following table. Code = round (Current (mA)/3.23).

Current (mA)	Code	BCHGISETDISCHARGEMSB	BCHGISETDISCHARGELSB
1340	≥415...511	≥207	1/0
800	248	124	0
400	124	62	0
268	0...≤83	≤41	1/0

Table 16: Discharge current limit

6.2.12 Electrical specification

Symbol	Description	Min.	Typ.	Max.	Unit
$VBAT_{POR}$	VBAT power-on reset release voltage		2.75		V
$VBAT_{BOR}$	VBAT brownout reset trigger		2.4		V
$V_{RECHARGE}$	Battery voltage level needed to restart charging, % of V_{TERM}		95		%
$V_{TERMACC}$	Accuracy of termination voltage	-1		+1	%
$I_{TRICKLE}$	Trickle charging current, % of I_{CHG}		10		%
I_{COOL}	Reduced charging current, % of I_{CHG}		50		%
$V_{TRICKLE\_FAST}$	Default threshold where trickle charging stops and constant current charging starts (register configurable)		2.9		V
$V_{CHDROPOUT}$	Charger dropout voltage		50		mV
$IBAT_{LIM}$	Output current limit for battery while discharging for code = 511		1340		mA
$RON_{CHARGER}$	Resistance between battery and VSYS		160		mΩ
$T_{CHGSTOP}$	Die temperature where charging stops (default)		110		°C
$T_{CHGRESUME}$	Die temperature where charging resumes (default)		100		°C
t_{REDECT}	Period between battery detection events		500		ms
$t_{OUTTRICKLE}$	Trickle charging timeout		10		min
$t_{OUTCHARGE}$	Constant current charging timeout		7		h

Table 17: Electrical specification

6.2.13 Electrical characteristics

The following graphs show CHARGER's electrical characteristics.

6.2.14 Registers

Instances

Instance	Base address	Description
BCHARGER	0x00000300	CHARGER Registers BCHARGER register map

Register overview

Register	Offset	Description
TASKRELEASEERR	0x0	Release Charger from Error
TASKCLEARCHGERR	0x1	Clear error registers

Register	Offset	Description
TASKCLEARSAFETYTIMER	0x2	Clear safety timers
BCHGENABLESET	0x4	Charger Enable Set
BCHGENABLECLR	0x5	Charger Enable Clear
BCHGDISABLESET	0x6	Charger Disable Recharge Set
BCHGDISABLECLR	0x7	Charger Disable Recharge Clear
BCHGISETMSB	0x8	Battery Charger Current Configuration
BCHGISETLSB	0x9	Battery Charger Current Configuration
BCHGISETDISCHARGEMSB	0xA	Battery Charger Discharge Configuration
BCHGISETDISCHARGELSB	0xB	Battery Charger Discharge Configuration
BCHGVTERM	0xC	Battery Charger Termination Voltage Normal temp
BCHGVTERMR	0xD	Battery Charger Termination Voltage Warm temp
BCHGVTRICKLESEL	0xE	Battery Charger Trickle Level Select
BCHGITERMSEL	0xF	Battery Charger ITERM Level Select
NTCCOLD	0x10	NTC threshold for COLD temperature region
NTCCOLDLSB	0x11	NTC threshold for COLD temperature region
NTCCOOL	0x12	NTC threshold for COOL temperature region
NTCCOOLLSB	0x13	NTC threshold for COOL temperature region
NTCWARM	0x14	NTC threshold for WARM temperature region
NTCWARMLSB	0x15	NTC threshold for WARM temperature region
NTCHOT	0x16	NTC threshold for HOT temperature region
NTCHOTLSB	0x17	NTC threshold for HOT temperature region
DIETEMPSTOP	0x18	DIE TEMP threshold for stop charging
DIETEMPSTOPLSB	0x19	DIE TEMP threshold for stop charging lsb
DIETEMPRESUME	0x1A	DIE TEMP threshold for resuming charging
DIETEMPRESUMELSB	0x1B	DIE TEMP threshold for resuming charging lsb
BCHGILIMSTATUS	0x2D	BCHARGER Ilim Status
NTCSTATUS	0x32	Ntc Comparator Status
DIETEMPSTATUS	0x33	DieTemp Comparator Status
BCHGCHARGESTATUS	0x34	Charging Status
BCHGERRREASON	0x36	Charger-FSM Error. Latched error reasons. Cleared with TASKS_CLEAR_CHG_ERR
BCHGERRSENSOR	0x37	Charger-FSM Error. Latched sensor values. Cleared with TASKS_CLEAR_CHG_ERR
BCHGCONFIG	0x3C	Charger configuration

6.2.14.1 TASKRELEASEERR

Address offset: 0x0

Release Charger from Error

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKRELEASEERROR			SW release from Charger Error state								
			NOEFFECT	0	No effect								
			TRIGGER	1	Trigger task								

6.2.14.2 TASKCLEARCHGERR

Address offset: 0x1

Clear error registers

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	W	TASKCLEARCHGERR			Clear registers BCHGERRREASON and BCHGERRSENSOR							
			NOEFFECT	0	No effect							
			TRIGGER	1	Trigger task							

6.2.14.3 TASKCLEARSAFETYTIMER

Address offset: 0x2

Clear safety timers

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	W	TASKCLEARSAFETYTIMER			Clear TRICKLE and CHARGE safety timers							
			NOEFFECT	0	No effect							
			TRIGGER	1	Trigger task							

6.2.14.4 BCHGENABLESET

Address offset: 0x4

Charger Enable Set

Bit number					7	6	5	4	3	2	1	0
ID											B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1S	ENABLECHARGING			Battery Charger Enable SET. (Read 0: Charging disabled). (Read 1: Charging enabled).							
			NOEFFECT	0	No effect							
			ENABLECHG	1	Enable Battery Charging							
B	RW W1S	ENABLEFULLCHGCOO			Battery Charger Enable Full Charge in Cool temp SET. (Read 0: 50% charge current value of BCHGISETMSB and BCHGISETLSB registers). (Read 1: 100% charge current value of BCHGISETMSB and BCHGISETLSB registers).							
			NOEFFECT	0	No effect							
			ENABLECOOL	1	Enable Charging of Cool battery							

6.2.14.5 BCHGENABLECLR

Address offset: 0x5

Charger Enable Clear

Bit number					7	6	5	4	3	2	1	0
ID											B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1C	ENABLECHARGING			Battery Charger Enable CLEAR. (Read 0: Charging disabled). (Read 1: Charging enabled).							
			NOEFFECT	0	No effect							
			DISABLECHG	1	Disable Battery Charging							
B	RW W1C	ENABLEFULLCHGCOC			Battery Charger Enable Full Charge in Cool temp CLEAR. (Read 0: 50% charge current value of BCHGISETMSB and BCHGISETLSB registers). (Read 1: 100% charge current value of BCHGISETMSB and BCHGISETLSB registers).							
			NOEFFECT	0	No effect							
			DISABLECOOL	1	Disable Charging of Cool battery							

6.2.14.6 BCHGDISABLESET

Address offset: 0x6

Charger Disable Recharge Set

Bit number					7	6	5	4	3	2	1	0
ID											B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1S	DISABLERECHARGE			Battery Charger Disable Recharge SET. (Read 0: Recharge enabled). (Read 1: Recharge disabled).							
			NOEFFECT	0	No effect							
			DISABLERCHG	1	Disable Recharging of battery once charged							
B	RW W1S	DISABLENTC			Battery Charger ignore NTC temperature limits SET. (Read 0: NTC values enabled) (Read 1: NTC values ignored)							
			NOEFFECT	0	No effect							
			IGNORENTC	1	Charging will ignore the NTC resistor measure							

6.2.14.7 BCHGDISABLECLR

Address offset: 0x7

Charger Disable Recharge Clear

Bit number					7	6	5	4	3	2	1	0
ID											B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1C	DISABLERECHARGE			Battery Charger Disable Recharge CLEAR. (Read 0: Recharge enabled). (Read 1: Recharge disabled).							
			NOEFFECT	0	No effect							
			ENABLERCHG	1	Enable Recharging of battery once charged							
B	RW W1C	DISABLENTC			Battery Charger ignore NTC temperature limits CLEAR. (Read 0: NTC values enabled). (Read 1: NTC values ignored).							
			NOEFFECT	0	No effect							
			USENTC	1	Charging will use the NTC resistor measure							

6.2.14.8 BCHGISETMSB

Address offset: 0x8

Battery Charger Current Configuration

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0x08						**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	BCHGISETCHARGEMSB			Battery Charger current setting (BCHG_ISET_CHARGE MSB bits [8:1]) default 32mA. See more from Charging Current chapter.								

6.2.14.9 BCHGISETLSB

Address offset: 0x9

Battery Charger Current Configuration

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	BCHGISETCHARGELSB			Battery Charger current fine tune by 2mA (BCHG_ISET_CHARGE LSB bit [0]). See more from Charging Current chapter.								

6.2.14.10 BCHGISETDISCHARGEMSB

Address offset: 0xA

Battery Charger Discharge Configuration

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0xCF						**1**	**1**	**0**	**0**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value	Description								
A	RW	BCHGISETDISCHARGEMSB			Battery Charger discharge current limiter (BCHG_ISET_DISCHARGE MSB bits [8:1]) default 1A limitation. See more from Discharge Current Limiter chapter.								

6.2.14.11 BCHGISETDISCHARGELSB

Address offset: 0xB

Battery Charger Discharge Configuration

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x01						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
ID	R/W	Field	Value ID	Value	Description								
A	RW	BCHGISETDISCHARGELSB			Battery Charger discharge current limiter fine tune (BCHG_ISET_DISCHARGE LSB bit [0]). See more from Discharge Current Limiter chapter.								

6.2.14.12 BCHGVTERM

Address offset: 0xC

Battery Charger Termination Voltage Normal temp

Bit number						7	6	5	4	3	2	1	0
ID										A	A	A	A
Reset 0x02						**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	BCHGVTERMNORM			Battery Charger Normal termination voltage. Values 14-15 are equals with default value(3V60).								
			3V50	0	3.50V								
			3V55	1	3.55V								
			3V60	2	3.60V(default)								
			3V65	3	3.65V								
			4V00	4	4.00V								
			4V05	5	4.05V								
			4V10	6	4.10V								
			4V15	7	4.15V								
			4V20	8	4.20V								
			4V25	9	4.25V								
			4V30	10	4.30V								
			4V35	11	4.35V								
			4V40	12	4.40V								
			4V45	13	4.45V								

6.2.14.13 BCHGVTERMR

Address offset: 0xD

Battery Charger Termination Voltage Warm temp

Bit number						7	6	5	4	3	2	1	0
ID										A	A	A	A
Reset 0x02						**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	BCHGVTERMREDUCED			Battery Charger Warm termination voltage. Values 14-15 are equals with default value(3V60).								
			3V50	0	3.50V								
			3V55	1	3.55V								
			3V60	2	3.60V(default)								
			3V65	3	3.65V								
			4V00	4	4.00V								
			4V05	5	4.05V								
			4V10	6	4.10V								
			4V15	7	4.15V								
			4V20	8	4.20V								
			4V25	9	4.25V								
			4V30	10	4.30V								
			4V35	11	4.35V								
			4V40	12	4.40V								
			4V45	13	4.45V								

6.2.14.14 BCHGVTRICKLESEL

Address offset: 0xE

Battery Charger Trickle Level Select

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	BCHGVTRICKLESEL			Battery Charger Vtrickle select								
			2V9	0	2.9V(default)								
			2V5	1	2.5V								

6.2.14.15 BCHGITERMSEL

Address offset: 0xF

Battery Charger ITERM Level Select

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	BCHGITERMSEL			Battery Charger ITERM select								
			SEL10	0	10%(default)								
			SEL20	1	20%								

6.2.14.16 NTCCOLD

Address offset: 0x10

NTC threshold for COLD temperature region

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0xBB						**1**	**0**	**1**	**1**	**1**	**0**	**1**	**1**
ID	R/W	Field	Value ID	Value	Description								
A	RW	NTCCOLDLVLMSB			NTC COLD level MSB bits								

6.2.14.17 NTCCOLDLSB

Address offset: 0x11

NTC threshold for COLD temperature region

Bit number						7	6	5	4	3	2	1	0
ID												A	A
Reset 0x01						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
ID	R/W	Field	Value ID	Value	Description								
A	RW	NTCCOLDLVLLSB			NTC COLD level LSB bits								

6.2.14.18 NTCCOOL

Address offset: 0x12

NTC threshold for COOL temperature region

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0xA4						**1**	**0**	**1**	**0**	**0**	**1**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	NTCCOOLLVLMSB			NTC COOL level MSB bits								

6.2.14.19 NTCCOOLLSB

Address offset: 0x13

NTC threshold for COOL temperature region

Bit number						7	6	5	4	3	2	1	0
ID												A	A
Reset 0x02						**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	NTCCOOLLVLLSB			NTC COOL level LSB bits								

6.2.14.20 NTCWARM

Address offset: 0x14

NTC threshold for WARM temperature region

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0x54						**0**	**1**	**0**	**1**	**0**	**1**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	NTCWARMLVLMSB			NTC WARM level MSB bits								

6.2.14.21 NTCWARMLSB

Address offset: 0x15

NTC threshold for WARM temperature region

Bit number						7	6	5	4	3	2	1	0
ID												A	A
Reset 0x01						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
ID	R/W	Field	Value ID	Value	Description								
A	RW	NTCWARMLVLLSB			NTC WARM level LSB bits								

6.2.14.22 NTCHOT

Address offset: 0x16

NTC threshold for HOT temperature region

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0x3B						**0**	**0**	**1**	**1**	**1**	**0**	**1**	**1**
ID	R/W	Field	Value ID	Value	Description								
A	RW	NTCHOTLVLMSB			NTC HOT level MSB bits								

6.2.14.23 NTCHOTLSB

Address offset: 0x17

NTC threshold for HOT temperature region

Bit number						7	6	5	4	3	2	1	0
ID												A	A
Reset 0x01						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
ID	R/W	Field	Value ID	Value	Description								
A	RW	NTCHOTLVLLSB			NTC HOT level LSB bits								

6.2.14.24 DIETEMPSTOP

Address offset: 0x18

DIE TEMP threshold for stop charging

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0x5A						**0**	**1**	**0**	**1**	**1**	**0**	**1**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	DIETEMPSTOPCHG			DIE TEMP STOP charging level								

6.2.14.25 DIETEMPSTOPLSB

Address offset: 0x19

DIE TEMP threshold for stop charging lsb

Bit number						7	6	5	4	3	2	1	0
ID												A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	DIETEMPSTOPCHGLSB			DIE TEMP STOP charging level Lsb bits								

6.2.14.26 DIETEMPRESUME

Address offset: 0x1A

DIE TEMP threshold for resuming charging

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0x5D						**0**	**1**	**0**	**1**	**1**	**1**	**0**	**1**
ID	R/W	Field	Value ID	Value	Description								
A	RW	DIETEMPRESUMECHG			DIE TEMP RESUME charging level								

6.2.14.27 DIETEMPRESUMELSB

Address offset: 0x1B

DIE TEMP threshold for resuming charging lsb

Bit number						7	6	5	4	3	2	1	0
ID												A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	DIETEMPRESUMECHGLSB			DIE TEMP RESUME charging level Lsb bits								

6.2.14.28 BCHGILIMSTATUS

Address offset: 0x2D

BCHARGER Ilim Status

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	R	BCHGILIMBATACTIVE			BCHARGER Ilimiter active								
			INACTIVE	0	Ilimbat not triggered								
			ACTIVE	1	Ilimbat triggered								

6.2.14.29 NTCSTATUS

Address offset: 0x32

Ntc Comparator Status

Bit number						7	6	5	4	3	2	1	0
ID										D	C	B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	R	NTCCOLD			Ntc Cold								
B	R	NTCCOOL			Ntc Cool								
C	R	NTCWARM			Ntc Warm								
D	R	NTCHOT			Ntc Hot								

6.2.14.30 DIETEMPSTATUS

Address offset: 0x33

DieTemp Comparator Status

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	R	DIETEMPHIGH			DieTemp High								
			NORMAL	0	Die below high threshold								
			HIGH	1	Die above high threshold								

6.2.14.31 BCHGCHARGESTATUS

Address offset: 0x34

Charging Status

Bit number					7	6	5	4	3	2	1	0
ID					H	G	F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	R	BATTERYDETECTED			Battery is connected							
B	R	COMPLETED			Charging completed (Battery Full)							
C	R	TRICKLECHARGE			Trickle charge							
D	R	CONSTANTCURRENT			Constant Current charging							
E	R	CONSTANTVOLTAGE			Constant Voltage charging							
F	R	RECHARGE			Battery re-charge is needed							
G	R	DIETEMPHIGHCHGPAUSED			Charging stopped due Die Temp high.							
H	R	SUPPLEMENTACTIVE			Supplement Mode Active							

6.2.14.32 BCHGERRREASON

Address offset: 0x36

Charger-FSM Error. Latched error reasons. Cleared with TASKS_CLEAR_CHG_ERR

Bit number					7	6	5	4	3	2	1	0
ID						G	F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	R	NTCSENSORERROR			Ntc sensor error							
B	R	VBATSENSORERROR			Vbat sensor error							
C	R	VBATLOW			VbatLow error							
D	R	VTRICKLE			Vtrickle error							
E	R	MEASTIMEOUT			Measurement timer timeout							
F	R	CHARGETIMEOUT			Charge timer timeout							
G	R	TRICKLETIMEOUT			Trickle timer timeout							

6.2.14.33 BCHGERRSENSOR

Address offset: 0x37

Charger-FSM Error. Latched sensor values. Cleared with TASKS_CLEAR_CHG_ERR

Bit number					7	6	5	4	3	2	1	0
ID					H	G	F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	R	SENSORNTCCOLD			Ntc Cold sensor value during error							
B	R	SENSORNTCCOOL			Ntc Cool sensor value during error							
C	R	SENSORNTCWARM			Ntc Warm sensor value during error							
D	R	SENSORNTCHOT			Ntc Hot sensor value during error							
E	R	SENSORVTERM			Vterm sensor value during error							
F	R	SENSORRECHARGE			Recharge sensor value during error							
G	R	SENSORVTRICKLE			Vtrickle sensor value during error							
H	R	SENSORVBATLOW			Vbatlow sensor value during error							

6.2.14.34 BCHGCONFIG

Address offset: 0x3C

Charger configuration

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	DISABLECHARGEWARM			Disable charging if battery is warm								
			ENABLED	0	Enable Charging if battery is warm								
			DISABLED	1	Disable Charging if battery is warm								

6.3 BUCK — Buck regulators

BUCK consists of two step-down buck regulators, BUCK1 and BUCK2.

BUCK[n] has the following features:

- Ultra-high efficiency (low IQ) and low noise operation
- PWM and Hysteretic modes with automatic switching based on load
- TWI configurable for forcing PWM mode to minimize output voltage ripple
- Configurable output voltages between 1.0 V and 3.3 V

Hysteretic mode offers efficiency at lower load currents and typically operates up to half the maximum PWM current. PWM mode provides a clean supply operation due to a constant switching frequency, F_{BUCK}. This provides optimal coexistence with RF circuits. BUCK can automatically change between Hysteretic and PWM modes.

6.3.1 On/Off control

BUCK is enabled in the following ways.

- **VSETn** pin
- Control registers
- GPIO pin

The **VSET1** and **VSET2** pins are enabled only at power-on. If resistor R_{VSETn} is present, BUCK is enabled with the output voltage defined by the resistor value. If the pin is grounded, BUCK is disabled. See Configuring default VOUT1 using an external resistor on page 42 and Configuring default VOUT2 using an external resistor on page 42.

Control registers BUCK1ENASET on page 45, BUCK1ENACLR on page 45, BUCK2ENASET on page 46, and BUCK2ENACLR on page 46 have enable and disable bits for each BUCK. These registers override the automatic BUCK enable or disable state.

A GPIO can be configured in register BUCKENCTRL on page 50 to enable or disable BUCK.

6.3.2 Output voltage selection

The output voltage range for BUCK[n] is programmable with TWI. The default output voltage selection is found on pins **VSET1** and **VSET2**, which are configured using an external resistor to **GND**. Pins **VSET1** and **VSET2** have two voltage configuration registers that are selectable through a GPIO pin with predefined voltage settings available.

The **VSET1** and **VSET2** pins are effective only at startup. The external resistor (maximum 5% tolerance) defines the default output voltage setting as found in the following table.

Symbol	Nominal resistance	Startup output voltage, VOUT1
R_{VSET1}	<100 Ω (grounded)	0 V (OFF)
	4.7 kΩ	1.0 V
	10 kΩ	1.2 V
	22 kΩ	1.5 V
	47 kΩ	1.8 V
	68 kΩ	2.0 V
	100 kΩ	2.2 V
	150 kΩ	2.5 V
	250...500 kΩ	2.7 V

Table 18: Configuring default VOUT1 using an external resistor

Symbol	Nominal resistance	Startup output voltage, VOUT2
R_{VSET2}	<100 Ω (grounded)	0 V (OFF)
	4.7 kΩ	1.8 V
	10 kΩ	2.0 V
	22 kΩ	2.2 V
	47 kΩ	2.4 V
	68 kΩ	2.5 V
	100 kΩ	2.7 V
	150 kΩ	3.0 V
	250...500 kΩ	3.3 V

Table 19: Configuring default VOUT2 using an external resistor

Note: Do not leave VSET1 or VSET2 floating.

If BUCK is disabled during power up, then the system defaults to software control of BUCK.

The output voltage range is from 1.0 V to 3.3 V in 100 mV steps and is set in the voltage configuration registers BUCK1NORMVOUT on page 47 and BUCK2NORMVOUT on page 48. Once the voltage is selected, register BUCKSWCTRLSEL on page 52 must be written to for the values to take effect.

Registers BUCK1VOUTSTATUS on page 52 and BUCK2VOUTSTATUS on page 52 indicate the status, or which voltage setting is currently selected.

A GPIO can be configured to select between two voltage levels. For example, a GPIO can be set to match the active/normal and retention/sleep states of the host. The output voltage for Retention mode is configured in registers BUCK1RETVOUT on page 48 and BUCK2RETVOUT on page 49. Select a GPIO to control retention voltage in register BUCKVRETCTRL on page 51

6.3.3 BUCK mode selection

BUCK operates in Automatic mode by default. When in Automatic mode, BUCK selects Hysteretic mode for low load currents, and PWM mode for high load currents.

This maximizes efficiency over the full range of supported load currents. In PWM mode, BUCK provides a clean supply operation due to constant switching frequency and lower voltage ripple for optimal coexistence with RF circuits.

Forced pulse width modulation (PWM) is set in the following ways:

- Control register bits BUCK1PWMSET on page 46 and BUCK2PWMSET on page 47
- GPIO pins

Register BUCKPWMCTRL on page 51 can configure a GPIO for PWM. It overrides the register setting for one or both BUCKs.

Automatic mode is most efficient over the whole load current range.

Hysteretic mode (PFM) can be forced in register BUCKCTRL0 on page 53 for each converter. This setting is not available using GPIO.

6.3.4 Active output capacitor discharge

Active discharge using R_{DISCH} from the output capacitors (when converter is disabled), can be enabled or disabled in register BUCKCTRL0 on page 53. The default setting is disabled.

Discharge of the capacitor is forced when there is a power cycle reset. See figure Power cycle on page 90.

6.3.5 Component selection

Recommended values for the inductor are shown in the following table.

Parameter	Value	Unit
Nominal inductance	2.2	µH
Inductor tolerance	≤ 20	%
DC resistance (DCR)	≤400	mΩ
Saturation current (I_{sat})	>350	mA
Rated current (I_{max})	>200	mA

Table 20: Inductor specifications

6.3.6 Electrical specification

Symbol	Description	Min.	Typ.	Max.	Unit
$VOUT1_{ACC}$ $VOUT2_{ACC}$	Output voltage accuracy	-5		+5	%
$VSYS_{MIN}$	Minimum VSYS voltage for enabling BUCK (Note)		2.7		V
I_{OUT}	PWM output current limit			400	mA

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DROP_OUT}	Drop-out voltage		200		mV
R_{DISCH}	Active output capacitor discharge resistance		2		kΩ
$I_{PWMTHRES}$	Load current threshold from Hysteretic to PWM mode (mode = AUTO)		90		mA
$I_{HYSTTHRES}$	Load current threshold from PWM to Hysteretic mode (mode = AUTO)		40		mA
$VOUT_{RIPPLEPWM}$	VOUT ripple in PWM mode (IOUT = 200 mA)		5		mVpp
$VOUT_{RIPPLEHYST}$	VOUT ripple in Hysteretic mode		50		mVpp
EFF_{BUCK}	Efficiency (VSYS=3.7 V, VOUT=1.8 V, IOUT=200 mA, PWM mode		93		%
f_{BUCK}	Switching frequency in PWM mode		3.6		MHz
t_{STRT}	Start-up time (VOUT=3.3V, C=10uF)		1.2		ms
$t_{PWMMODE}$	Transition time, Hysteretic to PWM mode, automatic (and via TWI or GPIO)		90 (55)		µs
t_{HYST}	Transition time, PWM to Hysteretic mode, automatic (and via TWI or GPIO)		35 (25)		µs
t_{SETTLE}	Settling time to within 1% after load transient from 0 mA to 200 mA		20		µs

Table 21: BUCK electrical specification

Note: Depends on VSYSCOMP setting.

6.3.7 Electrical Characteristics

The following graphs show BUCKs' electrical characteristics.

6.3.8 Registers

Instances

Instance	Base address	Description
BUCK	0x00000400	BUCK Registers BUCK register

Register overview

Register	Offset	Description
BUCK1ENASET	0x0	BUCK1 Enable pulse
BUCK1ENACLR	0x1	BUCK1 Disable pulse
BUCK2ENASET	0x2	BUCK2 Enable pulse
BUCK2ENACLR	0x3	BUCK2 Disable pulse
BUCK1PWMSET	0x4	BUCK1 PWM mode enable pulse
BUCK1PWMCLR	0x5	BUCK1 PWM mode disable pulse
BUCK2PWMSET	0x6	BUCK2 PWM mode enable pulse
BUCK2PWMCLR	0x7	BUCK2 PWM mode disable pulse
BUCK1NORMVOUT	0x8	BUCK1 Output voltage Normal mode
BUCK1RETVOUT	0x9	BUCK1 Output voltage Retention mode
BUCK2NORMVOUT	0xA	BUCK2 Output voltage Normal mode
BUCK2RETVOUT	0xB	BUCK2 Output voltage Retention mode
BUCKENCTRL	0xC	BUCK Enable GPIO Select
BUCKVRETCTRL	0xD	BUCK Retention Voltage select
BUCKPWMCTRL	0xE	BUCK Forced PWM mode GPIO select
BUCKSWCTRLSEL	0xF	BUCK Software Control select
BUCK1VOUTSTATUS	0x10	BUCK1 Vout Status register. Lets software read the Vout value in case its driven by the FSM.
BUCK2VOUTSTATUS	0x11	BUCK2 Vout Status register. Lets software read the Vout value in case its driven by the FSM.
BUCKCTRL0	0x15	BUCK Auto PFM to PWM Control select
BUCKSTATUS	0x34	BUCK status register

6.3.8.1 BUCK1ENASET

Address offset: 0x0

BUCK1 Enable pulse

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKBUCK1ENASET			Request to enable BUCK1								
			NOEFFECT	0	no effect								
			SET	1	BUCK1 Enable request set								

6.3.8.2 BUCK1ENACLR

Address offset: 0x1

BUCK1 Disable pulse

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKBUCK1ENACLR			Request to disable BUCK1								
			NOEFFECT	0	no effect								
			SET	1	BUCK1 Enable request clr								

6.3.8.3 BUCK2ENASET

Address offset: 0x2

BUCK2 Enable pulse

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKBUCK2ENASET			Request to enable BUCK2								
			NOEFFECT	0	no effect								
			SET	1	BUCK2 Enable request set								

6.3.8.4 BUCK2ENACLR

Address offset: 0x3

BUCK2 Disable pulse

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKBUCK2ENACLR			Request to enable BUCK2								
			NOEFFECT	0	no effect								
			SET	1	BUCK2 Enable request clr								

6.3.8.5 BUCK1PWMSET

Address offset: 0x4

BUCK1 PWM mode enable pulse

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKBUCK1PWMSET			request for BUCK1 to enter forced PWM mode								
			NOEFFECT	0	no effect								
			SET	1	BUCK1 Forced PWM request								

6.3.8.6 BUCK1PWMCLR

Address offset: 0x5

BUCK1 PWM mode disable pulse

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKBUCK1PWMCLR			request for BUCK1 to leave forced PWM mode and return to Auto mode								
			NOEFFECT	0	no effect								
			SET	1	BUCK1 Auto mode request								

6.3.8.7 BUCK2PWMSET

Address offset: 0x6

BUCK2 PWM mode enable pulse

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKBUCK2PWMSET			request for BUCK2 to enter forced PWM mode								
			NOEFFECT	0	no effect								
			SET	1	BUCK2 Forced PWM request								

6.3.8.8 BUCK2PWMCLR

Address offset: 0x7

BUCK2 PWM mode disable pulse

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKBUCK2PWMCLR			request for BUCK2 to leave forced PWM mode and return to Auto mode								
			NOEFFECT	0	no effect								
			SET	1	BUCK2 Auto mode request								

6.3.8.9 BUCK1NORMVOUT

Address offset: 0x8

BUCK1 Output voltage Normal mode

Bit number						7	6	5	4	3	2	1	0
ID									A	A	A	A	A
Reset 0x02						**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	BUCK1NORMVOUT			BUCK1 Output voltage Normal mode								
			1V	0	1V								
			1V1	1	1.1V								
			1V2	2	1.2V(Default)								
			1V3	3	1.3V								
			1V4	4	1.4V								
			1V5	5	1.5V								
			1V6	6	1.6V								
			1V7	7	1.7V								
			1V8	8	1.8V								
			1V9	9	1.9V								
			2V0	10	2V								
			2V1	11	2.1V								
			2V2	12	2.2V								
			2V3	13	2.3V								
			2V4	14	2.4V								
			2V5	15	2.5V								

Bit number						7	6	5	4	3	2	1	0
ID									A	A	A	A	A
Reset 0x02						**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
ID	R/W	Field	Value ID	Value	Description								
			2V6	16	2.6V								
			2V7	17	2.7V								
			2V8	18	2.8V								
			2V9	19	2.9V								
			3V0	20	3V								
			3V1	21	3.1V								
			3V2	22	3.2V								
			3V3	23	3.3V								
			3V30	24	3.3V								

6.3.8.10 BUCK1RETVOUT

Address offset: 0x9

BUCK1 Output voltage Retention mode

Bit number						7	6	5	4	3	2	1	0
ID									A	A	A	A	A
Reset 0x02						**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	BUCK1RETVOUT			BUCK1 Output voltage Retention mode								
			1V	0	1V								
			1V1	1	1.1V								
			1V2	2	1.2V(Default)								
			1V3	3	1.3V								
			1V4	4	1.4V								
			1V5	5	1.5V								
			1V6	6	1.6V								
			1V7	7	1.7V								
			1V8	8	1.8V								
			1V9	9	1.9V								
			2V0	10	2V								
			2V1	11	2.1V								
			2V2	12	2.2V								
			2V3	13	2.3V								
			2V4	14	2.4V								
			2V5	15	2.5V								
			2V6	16	2.6V								
			2V7	17	2.7V								
			2V8	18	2.8V								
			2V9	19	2.9V								
			3V0	20	3V								
			3V1	21	3.1V								
			3V2	22	3.2V								
			3V3	23	3.3V								
			3V30	24	3.3V								

6.3.8.11 BUCK2NORMVOUT

Address offset: 0xA

BUCK2 Output voltage Normal mode

Bit number						7	6	5	4	3	2	1	0
ID									A	A	A	A	A
Reset 0x08						**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	BUCK2NORMVOUT			BUCK2 Output voltage Normal mode								
			1V	0	1V								
			1V1	1	1.1V								
			1V2	2	1.2V								
			1V3	3	1.3V								
			1V4	4	1.4V								
			1V5	5	1.5V								
			1V6	6	1.6V								
			1V7	7	1.7V								
			1V8	8	1.8V(Default)								
			1V9	9	1.9V								
			2V0	10	2V								
			2V1	11	2.1V								
			2V2	12	2.2V								
			2V3	13	2.3V								
			2V4	14	2.4V								
			2V5	15	2.5V								
			2V6	16	2.6V								
			2V7	17	2.7V								
			2V8	18	2.8V								
			2V9	19	2.9V								
			3V0	20	3V								
			3V1	21	3.1V								
			3V2	22	3.2V								
			3V3	23	3.3V								
			3V30	24	3.3V								

6.3.8.12 BUCK2RETVOUT

Address offset: 0xB

BUCK2 Output voltage Retention mode

Bit number						7	6	5	4	3	2	1	0
ID									A	A	A	A	A
Reset 0x08						**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	BUCK2RETVOUT			BUCK2 Output voltage Retention mode								
			1V	0	1V								
			1V1	1	1.1V								
			1V2	2	1.2V								
			1V3	3	1.3V								
			1V4	4	1.4V								
			1V5	5	1.5V								
			1V6	6	1.6V								
			1V7	7	1.7V								
			1V8	8	1.8V(Default)								
			1V9	9	1.9V								

Bit number						7	6	5	4	3	2	1	0
ID									A	A	A	A	A
Reset 0x08						**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
			2V0	10	2V								
			2V1	11	2.1V								
			2V2	12	2.2V								
			2V3	13	2.3V								
			2V4	14	2.4V								
			2V5	15	2.5V								
			2V6	16	2.6V								
			2V7	17	2.7V								
			2V8	18	2.8V								
			2V9	19	2.9V								
			3V0	20	3V								
			3V1	21	3.1V								
			3V2	22	3.2V								
			3V3	23	3.3V								
			3V30	24	3.3V								

6.3.8.13 BUCKENCTRL

Address offset: 0xC

BUCK Enable GPIO Select

Bit number						7	6	5	4	3	2	1	0
ID						D	C	B	B	B	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	BUCK1ENGPISEL			Select which GPI controls BUCK1_enable								
			NOTUSED	0	Not used								
			GPIO0	1	GPI_0 selected								
			GPIO1	2	GPI_1 selected								
			GPIO2	3	GPI_2 selected								
			GPIO3	4	GPI_3 selected								
			GPIO4	5	GPI_4 selected								
			NOTUSED1	6	no GPI selected								
			NOTUSED2	7	no GPI selected								
B	RW	BUCK2ENGPISEL			Select which GPI controls BUCK2_enable								
			NOTUSED1	0	Not used								
			GPIO0	1	GPI_0 selected								
			GPIO1	2	GPI_1 selected								
			GPIO2	3	GPI_2 selected								
			GPIO3	4	GPI_3 selected								
			GPIO4	5	GPI_4 selected								
			NOTUSED3	6	no GPI selected								
			NOTUSED4	7	no GPI selected								
C	RW	BUCK1ENGPIINV			Invert the sense of the selected GPIO								
			NORMAL	0	not Inverted								
			INVERTED	1	Inverted								
D	RW	BUCK2ENGPIINV			Invert the sense of the selected GPIO								
			NORMAL	0	not Inverted								
			INVERTED	1	Inverted								

6.3.8.14 BUCKVRETCTRL

Address offset: 0xD

BUCK Retention Voltage select

Bit number						7	6	5	4	3	2	1	0
ID						D	C	B	B	B	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	BUCK1VRETGPISEL			Select which GPI controls BUCK1_retention voltage sel								
			NOTUSED	0	Not used								
			GPIO0	1	GPI_0 selected								
			GPIO1	2	GPI_1 selected								
			GPIO2	3	GPI_2 selected								
			GPIO3	4	GPI_3 selected								
			GPIO4	5	GPI_4 selected								
			NOTUSED2	6	Not used								
			NOTUSED1	7	Not used								
B	RW	BUCK2VRETGPISEL			Select which GPI controls BUCK2_retention voltage sel								
			NOTUSED	0	Not used								
			GPIO0	1	GPI_0 selected								
			GPIO1	2	GPI_1 selected								
			GPIO2	3	GPI_2 selected								
			GPIO3	4	GPI_3 selected								
			GPIO4	5	GPI_4 selected								
			NOTUSED2	6	Not used								
			NOTUSED1	7	Not used								
C	RW	BUCK1VRETGPIINV			Invert the sense of the selected GPIO								
			NORMAL	0	not Inverted								
			INVERTED	1	Inverted								
D	RW	BUCK2VRETGPIINV			Invert the sense of the selected GPIO								
			NORMAL	0	not Inverted								
			INVERTED	1	Inverted								

6.3.8.15 BUCKPWMCTRL

Address offset: 0xE

BUCK Forced PWM mode GPIO select

Bit number						7	6	5	4	3	2	1	0
ID						D	C	B	B	B	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	BUCK1PWMGPISEL			Select which GPI controls BUCK1 force PWM								
			NOTUSED1	0	Not used								
			GPIO0	1	GPI_0 selected								
			GPIO1	2	GPI_1 selected								
			GPIO2	3	GPI_2 selected								
			GPIO3	4	GPI_3 selected								
			GPIO4	5	GPI_4 selected								
			NOTUSED	6	Not used								
			NOTUSED2	7	Not used								
B	RW	BUCK2PWMGPISEL			Select which GPI controls BUCK2 force PWM								

Bit number						7	6	5	4	3	2	1	0
ID						D	C	B	B	B	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
			NOTUSED1	0	Not used								
			GPIO0	1	GPI_0 selected								
			GPIO1	2	GPI_1 selected								
			GPIO2	3	GPI_2 selected								
			GPIO3	4	GPI_3 selected								
			GPIO4	5	GPI_4 selected								
			NOTUSED	6	Not used								
			NOTUSED2	7	Not used								
C	RW	BUCK1PWMGPIINV			Invert the sense of the selected GPIO								
			NORMAL	0	not Inverted								
			INVERTED	1	Inverted								
D	RW	BUCK2PWMGPIINV			Invert the sense of the selected GPIO								
			NORMAL	0	not Inverted								
			INVERTED	1	Inverted								

6.3.8.16 BUCKSWCTRLSEL

Address offset: 0xF

BUCK Software Control select

Bit number						7	6	5	4	3	2	1	0
ID												B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	BUCK1SWCTRLSEL			BUCK1SwCtrlSel								
			VSETANDSWCTRL	0	Allow VSET pins to set VOUT								
			SWCTRL	1	Allow SW to override VSET pin								
B	RW	BUCK2SWCTRLSEL			BUCK2SwCtrlSel								
			VSETANDSWCTRL	0	Allow VSET pins to set VOUT								
			SWCTRL	1	Allow SW to override VSET pin								

6.3.8.17 BUCK1VOUTSTATUS

Address offset: 0x10

BUCK1 Vout Status register. Lets software read the Vout value in case its driven by the FSM.

Bit number						7	6	5	4	3	2	1	0
ID									A	A	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	R	BUCK1VOUTSTATUS			BUCK1VoutStatus								

6.3.8.18 BUCK2VOUTSTATUS

Address offset: 0x11

BUCK2 Vout Status register. Lets software read the Vout value in case its driven by the FSM.

Bit number						7	6	5	4	3	2	1	0
ID									A	A	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	R	BUCK2VOUTSTATUS			BUCK2VoutStatus								

6.3.8.19 BUCKCTRL0

Address offset: 0x15

BUCK Auto PFM to PWM Control select

Bit number						7	6	5	4	3	2	1	0
ID										D	C	B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	BUCK1AUTOCTRLSEL			BUCK1AutoCtrlSel								
			AUTO	0	Select Auto switching between PFM and PWM								
			PFM	1	Select PFM mode only								
B	RW	BUCK2AUTOCTRLSEL			BUCK2AutoCtrlSel								
			AUTO	0	Select Auto switching between PFM and PWM								
			PFM	1	Select PFM mode only								
C	RW	BUCK1ENPULLDOWN			BUCK1_EN_PULLDOWN								
			LOW	0	BUCK1 Pull Down Disabled								
			HIGH	1	BUCK1 Pull Down Enabled								
D	RW	BUCK2ENPULLDOWN			BUCK2_EN_PULLDOWN								
			LOW	0	BUCK2 Pull Down Disabled								
			HIGH	1	BUCK2 Pull Down Enabled								

6.3.8.20 BUCKSTATUS

Address offset: 0x34

BUCK status register

Bit number						7	6	5	4	3	2	1	0
ID						F	E	D	D	C	B	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	R	BUCK1MODE			BUCK1Mode								
			AUTOMODE	0	Auto mode								
			PFMMODE	1	PFM mode								
			PWMMODE	2	Force PWM mode								
B	R	BUCK1PWRGOOD			BUCK1PwrGood								
			BUCKDISABLED	0	BUCK powered off								
			BUCKPOWERED	1	BUCK powered on								
C	R	BUCK1PWMOK			BUCK1PwmOk								
			PWMMODEDISABLED	0	PWM mode disabled								
			PWMMODEENABLED	1	PWM mode enabled								
D	R	BUCK2MODE			BUCK2Mode								
			AUTOMODE	0	Auto mode								
			PFMMODE	1	PFM mode								
			PWMMODE	2	Force PWM mode								
E	R	BUCK2PWRGOOD			BUCK2PwrGood								
			BUCKDISABLED	0	BUCK powered off								

Bit number					7	6	5	4	3	2	1	0
ID					F	E	D	D	C	B	A	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
			BUCKPOWERED	1	BUCK powered on							
F	R	BUCK2PWMOK			BUCK2PwmOk							
			PWMMODEDISABLEI	0	PWM mode disabled							
			PWMMODEENABLEI	1	PWM mode enabled							

6.4 LOADSW/LDO — Load switches/LDO regulators

There are two load switches that can function as switches or LDOs. They have dedicated input pins that must have a voltage less than or equal to VSYS. The input voltage can be VOUT1, VOUT2, or any voltage up to VSYS.

The mode is selected using registers and .

Load switch

The switches are OFF by default and can be controlled in the following two ways.

- Control register bits for each load switch
  - TASKLDSW1SET on page 56
  - TASKLDSW1CLR on page 56
  - TASKLDSW2SET on page 56
  - TASKLDSW2CLR on page 57)
- GPIO pin(s), once configured by host software
  - LDSW1GPISEL on page 57
  - LDSW2GPISEL on page 58)

When a GPIO is configured for this purpose, it uses edges. When the GPIO toggles LOW to HIGH, the switch turns ON (conducting). When the GPIO toggles HIGH to LOW, the switch turns OFF.

Each load switch can be assigned to a separate GPIO, or a single GPIO can control both.

Soft start circuitry is enabled by host software and is adjustable. The soft start current limit can be set in a register up to 100 mA in 25 mA steps. A pull-down resistor R_{LSPD} at the **LSOUT** pin is enabled in a register bit. See register LDSWCONFIG on page 58.

If the load switch is supplied by an external source, the device will not provide current limiting. If the load switch is supplied from VBAT or VBUS, current limiting protects the system.

LDO mode

Both load switches can be separately configured as LDOs. The output voltage is configurable in registers and .

The LDO can be supplied from BUCK[n] or VSYS but must comply with VIN_{LDO}

6.4.1 Electrical specification

Symbol	Description	Min.	Typ.	Max.	Unit
$RDSON_{LS}$	Switch on-resistance (LS_{IN} = 3.3 V)		300		mΩ
I_{LS}	Current (LS_{OUT} ≥ 1.2 V)			100	mA
t_{SS}	Soft start time (soft start current limit = 25 mA, 10 µF, 0 V to 5 V)		1.8		ms
R_{LSPD}	Pull-down resistor (active discharge) at LS_{OUT}		2		kΩ
VIN_{LS}	Input voltage range	1.0		VSYS	V

Table 22: LOADSW electrical specification

Note: Minimum input voltage is defined by VOUT1 and VOUT2 including tolerances. The chip must be supplied by VBAT or VBUS before inputting voltage to the load switch.

Symbol	Description	Min.	Typ.	Max.	Unit
$IOUT_{LDO}$	Output current VOUT > 1.2 V			50	mA
$IOUT_{LDO}$	Output current VOUT < 1.2 V			10	mA
VIN_{LDO}	Input voltage range	2.6		VSYS	V
$VOUT_{LDO}$	Minimum setting output voltage		1.0		V
$VOUT_{LDO}$	Maximum setting output voltage		3.3		V
$VOUT_{LDO}$ step	Output voltage step size		100		mV
t_{STRTUP}	Start-up time ($VOUT_{LDO}$=1.8V, 20 µF, IOUT=0)				µs
$VDROP_{LDO}$	Drop-out voltage ($IOUT_{LDO}$=50 mA, VOUTLDO=3.3 V)		200		mV

Table 23: LDO electrical specification

6.4.2 Electrical characteristics

The following graphs show LOADSW's electrical characteristics.

6.4.3 Registers

Instances

Instance	Base address	Description
LDSW	0x00000800	LOADSW Registers
		LDSW register map

Register overview

Register	Offset	Description
TASKLDSW1SET	0x0	Enable LDSW1
TASKLDSW1CLR	0x1	Disable LDSW1
TASKLDSW2SET	0x2	Enable LDSW2
TASKLDSW2CLR	0x3	Disable LDSW2
LDSWSTATUS	0x4	Load Switch Status
LDSW1GPISEL	0x5	Load Switch1 GPIO Control Select
LDSW2GPISEL	0x6	Load Switch2 GPIO Control Select
LDSWCONFIG	0x7	Load Switch Configuration

6.4.3.1 TASKLDSW1SET

Address offset: 0x0

Enable LDSW1

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKLDSW1SET			LDSW1_Enable request SET								
			NOEFFECT	0	no effect								
			SET	1	LDSW1 Enable request set								

6.4.3.2 TASKLDSW1CLR

Address offset: 0x1

Disable LDSW1

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKLDSW1CLR			LDSW1_Enable request CLR								
			NOEFFECT	0	no effect								
			CLR	1	LDSW1 Disable request clr								

6.4.3.3 TASKLDSW2SET

Address offset: 0x2

Enable LDSW2

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKLDSW2SET			LDSW2_Enable request SET								
			NOEFFECT	0	no effect								
			SET	1	LDSW2 Enable request set								

6.4.3.4 TASKLDSW2CLR

Address offset: 0x3

Disable LDSW2

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKLDSW2CLR			LDSW2_Enable request CLR								
			NOEFFECT	0	no effect								
			CLR	1	LDSW2 Disable request clr								

6.4.3.5 LDSWSTATUS

Address offset: 0x4

Load Switch Status

Bit number						7	6	5	4	3	2	1	0
ID									E	D	C	B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	R	LDSW1PWRUPLDSW			Power up signal to move load switch 1 into and out of load switch state. When the load switch is enabled the low-dropout regulator is disabled. This is ensured by digital logic.								
B	R	LDSW1PWRUPLDO			Power up signal to move low-dropout regulator 1into and out of low-dropout active state. When the low-dropout regulator is enabled the load switch is disabled.								
C	R	LDSW2PWRUPLDSW			Power up signal to move low-dropout regulator 2 into and out of low-dropout active state. When the low-dropout regulator is enabled the load switch is disabled. This is ensured by digital logic.								
D	R	LDSW2PWRUPLDO			Load switch 2 softstart causes passfet to deliver a constant current from LS2_IN to LS2_OUT. It brings the load switch into and out of the sofstart state.								
E	R	LDSWENABLE			Enable signal to move the overal load switch + low-dropout regulator IP from Awake to Deepsleep state to save power when required.								

6.4.3.6 LDSW1GPISEL

Address offset: 0x5

Load Switch1 GPIO Control Select

Bit number						7	6	5	4	3	2	1	0
ID										B	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	LDSW1GPISEL			Select which GPI controls Load Switch1								
			NOTUSED1	0	no GPI selected								
			GPIO0	1	GPI_0 selected								
			GPIO1	2	GPI_1 selected								
			GPIO2	3	GPI_2 selected								
			GPIO3	4	GPI_3 selected								

Bit number					7	6	5	4	3	2	1	0
ID									B	A	A	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
			GPIO4	5	GPI_4 selected							
			NOTUSED2	6	no GPI selected							
			NOTUSED3	7	no GPI selected							
B	RW	LDSW1GPIINV			Invert the sense of the selected GPIO							
			NORMAL	0	not Inverted							
			INVERTED	1	Inverted							

6.4.3.7 LDSW2GPISEL

Address offset: 0x6

Load Switch2 GPIO Control Select

Bit number					7	6	5	4	3	2	1	0
ID									B	A	A	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	LDSW2GPISEL			Select which GPI controls Load Switch2							
			NOTUSED1	0	no GPI selected							
			GPIO0	1	GPI_0 selected							
			GPIO1	2	GPI_1 selected							
			GPIO2	3	GPI_2 selected							
			GPIO3	4	GPI_3 selected							
			GPIO4	5	GPI_4 selected							
			NOTUSED2	6	no GPI selected							
			NOTUSED3	7	no GPI selected							
B	RW	LDSW2GPIINV			Invert the sense of the selected GPIO							
			NORMAL	0	not Inverted							
			INVERTED	1	Inverted							

6.4.3.8 LDSWCONFIG

Address offset: 0x7

Load Switch Configuration

Bit number					7	6	5	4	3	2	1	0
ID					F	E	D	D	C	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	LDSW1SOFTSTARTDISABLE			Load Switch1 Soft Start Disable							
			NOEFFECT	0	no effect							
			NOSOFTSTART	1	Soft Start Disabled							
B	RW	LDSW2SOFTSTARTDI			Load Switch2 Soft Start Disable							
			NOEFFECT	0	no effect							
			NOSOFTSTART	1	Soft Start Disabled							
C	RW	LDSW1SOFTSTARTSEL			Select Soft Start level for Load Switch1							
			25mA	0	25mA							
			50mA	1	50mA							
			75mA	2	75mA							
			100mA	3	100mA							

Bit number						7	6	5	4	3	2	1	0
ID						F	E	D	D	C	C	B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
D	RW	LDSW2SOFTSTARTSE			Select Soft Start level for Load Switch1								
			25mA	0	25mA								
			50mA	1	50mA								
			75mA	2	75mA								
			100mA	3	100mA								
E	RW	LDSW1ACTIVEDISCHARGE			Load Switch1 Active discharge Enable								
			NODISCHARGE	0	No Discharge								
			ACTIVE	1	Active Discharge Enabled								
F	RW	LDSW2ACTIVEDISCH/			Load Switch2 Active discharge Enable								
			NODISCHARGE	0	No Discharge								
			ACTIVE	1	Active Discharge Enabled								

6.5 LEDDRV — LED drivers

LEDDRV is made of three identical low-side LED drivers on pins **LED0**, **LED1**, and **LED2**. They can be configured in registers to be one of the following LED types:

- Charging indication
- Charging error indication
- An RGB LED (requires all three pins)
- A general purpose, open-drain output

The pin configurations are independent of each other. When used as charging indications, the charging state machine controls LEDDRV.

When used as general purpose LED drivers, a control register contains separate bits for enabling each driver, see registers LEDDRV0SET on page 61 and LEDDRV0CLR on page 61. The host software will set or reset the control register bit which alters the state of the LED associated with that register bit.

LEDDRV can be used as open-drain digital output. Open Drain mode is the same as the general purpose LED drivers but with the LED removed. An external pull up resistor is required for each LED pin operating in Open Drain mode.

The system can control an RGB LED. The common anode LED has the common anode connected to a supply that is lower than VSYS voltage. The R, G, and B connections are linked to LED0, LED1, and LED2, in no particular order. The R, G, or B is activated by enabling the associated LED register. Combinations of RG, RB, GB, and RGB are possible.

6.5.1 Electrical specification

Symbol	Description	Min.	Typ.	Max.	Unit
I_{LED}	LED driver current		5		mA
V_{LEDn}	Voltage on pin LED0, LED1 and LED2	0.5		VSYS	V

Table 24: LEDDRV electrical specification

6.5.2 Registers

Instances

Instance	Base address	Description
LEDDRV	0x00000A00	LEVDRV Registers LEDDRV register map

Register overview

Register	Offset	Description
LEDDRV0MODESEL	0x0	Select for LED_0 mode
LEDDRV1MODESEL	0x1	Select for LED_1 mode
LEDDRV2MODESEL	0x2	Select for LED_2 mode
LEDDRV0SET	0x3	Set LED_0 to be On
LEDDRV0CLR	0x4	Clear LED_0 to be Off
LEDDRV1SET	0x5	Set LED_1 to be On
LEDDRV1CLR	0x6	Clear LED_1 to be Off
LEDDRV2SET	0x7	Set LED_2 to be On
LEDDRV2CLR	0x8	Clear LED_2 to be Off

6.5.2.1 LEDDRV0MODESEL

Address offset: 0x0

Select for LED_0 mode

Bit number						7	6	5	4	3	2	1	0
ID												A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	LEDDRV0MODESEL			Select for LED_0 mode								
			ERROR	0	Error condition from Charger								
			CHARGING	1	Charging indicator (On during charging)								
			HOST	2	Driven from register LEDDRV_0_SET/CLR								
			NOTUSED	3	Not used								

6.5.2.2 LEDDRV1MODESEL

Address offset: 0x1

Select for LED_1 mode

Bit number						7	6	5	4	3	2	1	0
ID												A	A
Reset 0x01						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
ID	R/W	Field	Value ID	Value	Description								
A	RW	LEDDRV1MODESEL			Select for LED_1 mode								
			ERROR	0	Error condition from Charger								
			CHARGING	1	Charging indicator (On during charging)								
			HOST	2	Driven from register LEDDRV_1_SET/CLR								
			NOTUSED	3	Not used								

6.5.2.3 LEDDRV2MODESEL

Address offset: 0x2

Select for LED_2 mode

Bit number						7	6	5	4	3	2	1	0
ID												A	A
Reset 0x02						**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	LEDDRV2MODESEL			Select for LED_2 mode								
			ERROR	0	Error condition from Charger								
			CHARGING	1	Charging indicator (On during charging)								
			HOST	2	Driven from register LEDDRV_2_SET/CLR								
			NOTUSED	3	Not used								

6.5.2.4 LEDDRV0SET

Address offset: 0x3

Set LED_0 to be On

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	LEDDRV0ON			Set LED_0 to be On								
			NOEFFECT	0	no effect								
			SET	1	Used with leddrvModeSel								

6.5.2.5 LEDDRV0CLR

Address offset: 0x4

Clear LED_0 to be Off

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	LEDDRV0OFF			Set LED_0 to be Off								
			NOEFFECT	0	no effect								
			CLR	1	Used with leddrvModeSel								

6.5.2.6 LEDDRV1SET

Address offset: 0x5

Set LED_1 to be On

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	LEDDRV1ON			Set LED_1 to be On								
			NOEFFECT	0	no effect								
			SET	1	Used with leddrvModeSel								

6.5.2.7 LEDDRV1CLR

Address offset: 0x6

Clear LED_1 to be Off

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	LEDDRV1OFF			Set LED_1 to be Off								
			NOEFFECT	0	no effect								
			CLR	1	Used with leddrvModeSel								

6.5.2.8 LEDDRV2SET

Address offset: 0x7

Set LED_2 to be On

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	LEDDRV2ON			Set LED_2 to be On								
			NOEFFECT	0	no effect								
			SET	1	Used with leddrvModeSel								

6.5.2.9 LEDDRV2CLR

Address offset: 0x8

Clear LED_2 to be Off

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	LEDDRV2OFF			Set LED_2 to be Off								
			NOEFFECT	0	no effect								
			CLR	1	Used with leddrvModeSel								

6.6 GPIO — General purpose input/output

The general purpose input/output pins (GPIOs) are set as input with weak pull-down by default and supplied by VDDIO.

The number of GPIOs may vary with product variant and package. See Pin assignments on page 127 for more information about the number of supported GPIOs.

Pins can be configured by the host software to function as control input, general purpose input, and output.

Note: Events may occur when GPIO configuration is changed on the fly.

Pull-down is prioritized if both pull-up and pull-down are activated for a GPIO at the same time.

The following figure shows BUCK control. The system can be set up for a GPIO to control BUCK[n] and LOADSW[n].

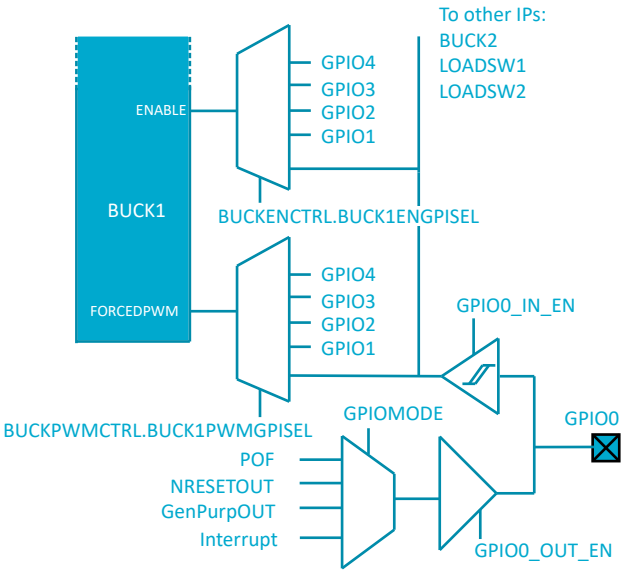

Figure 6: GPIO concept

Pins **LED0**, **LED1**, and **LED2** can be used as open-drain outputs, see LEDDRV — LED drivers on page 59.

6.6.1 Control input

For a pin to function as a control input, select `GPI Input` in one of the GPIOMODE[n] registers and then configure the feature as follows.

- LOADSW[n] enable – select the corresponding GPIO in register LDSW1GPISEL on page 57 or register LDSW2GPISEL on page 58
- BUCK[n] enable – select the corresponding GPIO in register BUCKENCTRL on page 50
- BUCK[n] forced PWM mode – select the corresponding GPIO in register BUCKPWMCTRL on page 51
- BUCK[n] VOUT[n] voltage level selection for active and retention/sleep modes – select the corresponding GPIO in register BUCKVRETCTRL on page 51
- Second reset button – GPIO0 only (see Two-button reset on page 98)

6.6.2 General purpose input

These modes are configured in one of the GPIOMODE[0] on page 65- GPIOMODE[4] on page 67 registers as described below:

- General purpose input not generating event register activity. Select "GPI Input".
- General purpose input generating an event on rising or falling edge. Select "GPI Rising Edge Event" or "GPI Falling Edge Event", respectively. The events are visible in EVENTSGPIOSET on page 119
- Overriding GPIO input states can be done using "GPI Logic1" and "GPI Logic0"

6.6.3 Output

Output is configured in registers GPIOMODE[0] on page 65 - GPIOMODE[4] on page 67 and described as the following:

- Interrupt towards the host: select "GPO Interrupt"
- Reset output (NRESETOUT from watchdog, active low). Select "GPO Reset"
- Power fail (POF) warning: select "GPO PowerLossWarn"
- General purpose output: select "GPO Logic1" or "GPO Logic0" to output high or low level, respectively

Drive strength can be selected between 1 mA (default) and 6 mA. Weak pull-up and pull-down resistors are available. Open-drain operation and input debouncing is also available: GPIODRIVE[0] on page 67, GPIODEBOUNCE[0] on page 72, GPIOPDEN[0] on page 70, GPIOPUEN[0] on page 68 and GPIOOPENDRAIN[0] on page 71.

6.6.4 Electrical specification

Symbol	Description	Min.	Typ.	Max.	Unit
V_{IH}	Input high voltage	0.7 x VDDIO		VDDIO	V
V_{IL}	Input low voltage	AVSS		0.3 x VDDIO	V
PU_{GPIO}	Weak pull-up resistor		500		kΩ
PD_{GPIO}	Weak pull-down resistor		500		kΩ
DB_{GPIO}	Input debounce time (DEBOUNCE1=1)		20		ms

Table 25: GPIO electrical specification

6.6.5 Registers

Instances

Instance	Base address	Description
GPIOS	0x00000600	GPIO Registers GPIOS register map

Register overview

Register	Offset	Description
GPIOMODE[0]	0x0	GPIO Mode Configuration
GPIOMODE[1]	0x1	GPIO Mode Configuration
GPIOMODE[2]	0x2	GPIO Mode Configuration
GPIOMODE[3]	0x3	GPIO Mode Configuration
GPIOMODE[4]	0x4	GPIO Mode Configuration
GPIODRIVE[0]	0x5	GPIO Drive strength Configuration
GPIODRIVE[1]	0x6	GPIO Drive strength Configuration
GPIODRIVE[2]	0x7	GPIO Drive strength Configuration
GPIODRIVE[3]	0x8	GPIO Drive strength Configuration
GPIODRIVE[4]	0x9	GPIO Drive strength Configuration
GPIOPUEN[0]	0xA	GPIO Pull-up Enable Configuration

Register	Offset	Description
GPIOPUEN[1]	0xB	GPIO Pull-up Enable Configuration
GPIOPUEN[2]	0xC	GPIO Pull-up Enable Configuration
GPIOPUEN[3]	0xD	GPIO Pull-up Enable Configuration
GPIOPUEN[4]	0xE	GPIO Pull-up Enable Configuration
GPIOPDEN[0]	0xF	GPIO Pull-down Enable Configuration
GPIOPDEN[1]	0x10	GPIO Pull-down Enable Configuration
GPIOPDEN[2]	0x11	GPIO Pull-down Enable Configuration
GPIOPDEN[3]	0x12	GPIO Pull-down Enable Configuration
GPIOPDEN[4]	0x13	GPIO Pull-down Enable Configuration
GPIOOPENDRAIN[0]	0x14	GPIO Open Drain Configuration
GPIOOPENDRAIN[1]	0x15	GPIO Open Drain Configuration
GPIOOPENDRAIN[2]	0x16	GPIO Open Drain Configuration
GPIOOPENDRAIN[3]	0x17	GPIO Open Drain Configuration
GPIOOPENDRAIN[4]	0x18	GPIO Open Drain Configuration
GPIODEBOUNCE[0]	0x19	GPIO Debounce Configuration
GPIODEBOUNCE[1]	0x1A	GPIO Debounce Configuration
GPIODEBOUNCE[2]	0x1B	GPIO Debounce Configuration
GPIODEBOUNCE[3]	0x1C	GPIO Debounce Configuration
GPIODEBOUNCE[4]	0x1D	GPIO Debounce Configuration
GPIOSTATUS	0x1E	GPIO Status from GPIO Pads

6.6.5.1 GPIOMODE[0]

Address offset: 0x0

GPIO Mode Configuration

Bit number						7	6	5	4	3	2	1	0
ID										A	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	GPIOMODE			Config for GPIO mode selection								
			GPIINPUT	0	GPI Input								
			GPILOGIC1	1	GPI Logic1								
			GPILOGIC0	2	GPI Logic0								
			GPIEVENTRISE	3	GPI Rising Edge Event								
			GPIEVENTFALL	4	GPI Falling Edge Event								
			GPOIRQ	5	GPO Interrupt								
			GPORESET	6	GPO Reset								
			GPOPLW	7	GPO PwrLossWarn								
			GPOLOGIC1	8	GPO Logic1								
			GPOLOGIC0	9	GPO Logic0								

6.6.5.2 GPIOMODE[1]

Address offset: 0x1

GPIO Mode Configuration

Bit number						7	6	5	4	3	2	1	0
ID										A	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	GPIOMODE			Config for GPIO mode selection								

Bit number						7	6	5	4	3	2	1	0
ID										A	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
			GPIINPUT	0	GPI Input								
			GPILOGIC1	1	GPI Logic1								
			GPILOGIC0	2	GPI Logic0								
			GPIEVENTRISE	3	GPI Rising Edge Event								
			GPIEVENTFALL	4	GPI Falling Edge Event								
			GPOIRQ	5	GPO Interrupt								
			GPORESET	6	GPO Reset								
			GPOPLW	7	GPO PwrLossWarn								
			GPOLOGIC1	8	GPO Logic1								
			GPOLOGIC0	9	GPO Logic0								

6.6.5.3 GPIOMODE[2]

Address offset: 0x2

GPIO Mode Configuration

Bit number						7	6	5	4	3	2	1	0
ID										A	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	GPIOMODE			Config for GPIO mode selection								
			GPIINPUT	0	GPI Input								
			GPILOGIC1	1	GPI Logic1								
			GPILOGIC0	2	GPI Logic0								
			GPIEVENTRISE	3	GPI Rising Edge Event								
			GPIEVENTFALL	4	GPI Falling Edge Event								
			GPOIRQ	5	GPO Interrupt								
			GPORESET	6	GPO Reset								
			GPOPLW	7	GPO PwrLossWarn								
			GPOLOGIC1	8	GPO Logic1								
			GPOLOGIC0	9	GPO Logic0								

6.6.5.4 GPIOMODE[3]

Address offset: 0x3

GPIO Mode Configuration

Bit number						7	6	5	4	3	2	1	0
ID										A	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	GPIOMODE			Config for GPIO mode selection								
			GPIINPUT	0	GPI Input								
			GPILOGIC1	1	GPI Logic1								
			GPILOGIC0	2	GPI Logic0								
			GPIEVENTRISE	3	GPI Rising Edge Event								
			GPIEVENTFALL	4	GPI Falling Edge Event								
			GPOIRQ	5	GPO Interrupt								
			GPORESET	6	GPO Reset								

Bit number						7	6	5	4	3	2	1	0
ID										A	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
			GPOPLW	7	GPO PwrLossWarn								
			GPOLOGIC1	8	GPO Logic1								
			GPOLOGIC0	9	GPO Logic0								

6.6.5.5 GPIOMODE[4]

Address offset: 0x4

GPIO Mode Configuration

Bit number						7	6	5	4	3	2	1	0
ID										A	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	GPIOMODE			Config for GPIO mode selection								
			GPIINPUT	0	GPI Input								
			GPILOGIC1	1	GPI Logic1								
			GPILOGIC0	2	GPI Logic0								
			GPIEVENTRISE	3	GPI Rising Edge Event								
			GPIEVENTFALL	4	GPI Falling Edge Event								
			GPOIRQ	5	GPO Interrupt								
			GPORESET	6	GPO Reset								
			GPOPLW	7	GPO PwrLossWarn								
			GPOLOGIC1	8	GPO Logic1								
			GPOLOGIC0	9	GPO Logic0								

6.6.5.6 GPIODRIVE[0]

Address offset: 0x5

GPIO Drive strength Configuration

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	GPIODRIVE			Config for GPIO drive strength								
			1MA	0	1mA								
			6MA	1	6mA								

6.6.5.7 GPIODRIVE[1]

Address offset: 0x6

GPIO Drive strength Configuration

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	GPIODRIVE			Config for GPIO drive strength							
			1MA	0	1mA							
			6MA	1	6mA							

6.6.5.8 GPIODRIVE[2]

Address offset: 0x7

GPIO Drive strength Configuration

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	GPIODRIVE			Config for GPIO drive strength							
			1MA	0	1mA							
			6MA	1	6mA							

6.6.5.9 GPIODRIVE[3]

Address offset: 0x8

GPIO Drive strength Configuration

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	GPIODRIVE			Config for GPIO drive strength							
			1MA	0	1mA							
			6MA	1	6mA							

6.6.5.10 GPIODRIVE[4]

Address offset: 0x9

GPIO Drive strength Configuration

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	GPIODRIVE			Config for GPIO drive strength							
			1MA	0	1mA							
			6MA	1	6mA							

6.6.5.11 GPIOPUEN[0]

Address offset: 0xA

GPIO Pull-up Enable Configuration

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	GPIOPUEN			Config for GPIO pull-up enable							
			PULLUP0	0	Pull Up Disable							
			PULLUP1	1	Pull Up Enable							

6.6.5.12 GPIOPUEN[1]

Address offset: 0xB

GPIO Pull-up Enable Configuration

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	GPIOPUEN			Config for GPIO pull-up enable							
			PULLUP0	0	Pull Up Disable							
			PULLUP1	1	Pull Up Enable							

6.6.5.13 GPIOPUEN[2]

Address offset: 0xC

GPIO Pull-up Enable Configuration

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	GPIOPUEN			Config for GPIO pull-up enable							
			PULLUP0	0	Pull Up Disable							
			PULLUP1	1	Pull Up Enable							

6.6.5.14 GPIOPUEN[3]

Address offset: 0xD

GPIO Pull-up Enable Configuration

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	GPIOPUEN			Config for GPIO pull-up enable							
			PULLUP0	0	Pull Up Disable							
			PULLUP1	1	Pull Up Enable							

6.6.5.15 GPIOPUEN[4]

Address offset: 0xE

GPIO Pull-up Enable Configuration

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	GPIOPUEN			Config for GPIO pull-up enable								
			PULLUP0	0	Pull Up Disable								
			PULLUP1	1	Pull Up Enable								

6.6.5.16 GPIOPDEN[0]

Address offset: 0xF

GPIO Pull-down Enable Configuration

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x01						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
ID	R/W	Field	Value ID	Value	Description								
A	RW	GPIOPDEN			Config for GPIO pull-down enable								
			PULLDOWN0	0	Pull Down Disable								
			PULLDOWN1	1	Pull Down Enable								

6.6.5.17 GPIOPDEN[1]

Address offset: 0x10

GPIO Pull-down Enable Configuration

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x01						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
ID	R/W	Field	Value ID	Value	Description								
A	RW	GPIOPDEN			Config for GPIO pull-down enable								
			PULLDOWN0	0	Pull Down Disable								
			PULLDOWN1	1	Pull Down Enable								

6.6.5.18 GPIOPDEN[2]

Address offset: 0x11

GPIO Pull-down Enable Configuration

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x01						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
ID	R/W	Field	Value ID	Value	Description								
A	RW	GPIOPDEN			Config for GPIO pull-down enable								
			PULLDOWN0	0	Pull Down Disable								
			PULLDOWN1	1	Pull Down Enable								

6.6.5.19 GPIOPDEN[3]

Address offset: 0x12

GPIO Pull-down Enable Configuration

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x01					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
ID	R/W	Field	Value ID	Value	Description							
A	RW	GPIOPDEN			Config for GPIO pull-down enable							
			PULLDOWN0	0	Pull Down Disable							
			PULLDOWN1	1	Pull Down Enable							

6.6.5.20 GPIOPDEN[4]

Address offset: 0x13

GPIO Pull-down Enable Configuration

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x01					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
ID	R/W	Field	Value ID	Value	Description							
A	RW	GPIOPDEN			Config for GPIO pull-down enable							
			PULLDOWN0	0	Pull Down Disable							
			PULLDOWN1	1	Pull Down Enable							

6.6.5.21 GPIOOPENDRAIN[0]

Address offset: 0x14

GPIO Open Drain Configuration

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	GPIOOPENDRAIN			Config for GPIO open drain							
			OPENDRAIN0	0	Open Drain Disable							
			OPENDRAIN1	1	Open Drain Enable							

6.6.5.22 GPIOOPENDRAIN[1]

Address offset: 0x15

GPIO Open Drain Configuration

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	GPIOOPENDRAIN			Config for GPIO open drain							
			OPENDRAIN0	0	Open Drain Disable							
			OPENDRAIN1	1	Open Drain Enable							

6.6.5.23 GPIOOPENDRAIN[2]

Address offset: 0x16

GPIO Open Drain Configuration

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	GPIOOPENDRAIN			Config for GPIO open drain							
			OPENDRAIN0	0	Open Drain Disable							
			OPENDRAIN1	1	Open Drain Enable							

6.6.5.24 GPIOOPENDRAIN[3]

Address offset: 0x17

GPIO Open Drain Configuration

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	GPIOOPENDRAIN			Config for GPIO open drain							
			OPENDRAIN0	0	Open Drain Disable							
			OPENDRAIN1	1	Open Drain Enable							

6.6.5.25 GPIOOPENDRAIN[4]

Address offset: 0x18

GPIO Open Drain Configuration

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	GPIOOPENDRAIN			Config for GPIO open drain							
			OPENDRAIN0	0	Open Drain Disable							
			OPENDRAIN1	1	Open Drain Enable							

6.6.5.26 GPIODEBOUNCE[0]

Address offset: 0x19

GPIO Debounce Configuration

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	GPIODEBOUNCE			Config for GPIO debounce							
			DEBOUNCE0	0	Debounce Disable							
			DEBOUNCE1	1	Debounce Enable							

6.6.5.27 GPIODEBOUNCE[1]

Address offset: 0x1A

GPIO Debounce Configuration

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	GPIODEBOUNCE			Config for GPIO debounce							
			DEBOUNCE0	0	Debounce Disable							
			DEBOUNCE1	1	Debounce Enable							

6.6.5.28 GPIODEBOUNCE[2]

Address offset: 0x1B

GPIO Debounce Configuration

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	GPIODEBOUNCE			Config for GPIO debounce							
			DEBOUNCE0	0	Debounce Disable							
			DEBOUNCE1	1	Debounce Enable							

6.6.5.29 GPIODEBOUNCE[3]

Address offset: 0x1C

GPIO Debounce Configuration

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	GPIODEBOUNCE			Config for GPIO debounce							
			DEBOUNCE0	0	Debounce Disable							
			DEBOUNCE1	1	Debounce Enable							

6.6.5.30 GPIODEBOUNCE[4]

Address offset: 0x1D

GPIO Debounce Configuration

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	GPIODEBOUNCE			Config for GPIO debounce							
			DEBOUNCE0	0	Debounce Disable							
			DEBOUNCE1	1	Debounce Enable							

6.6.5.31 GPIOSTATUS

Address offset: 0x1E

GPIO Status from GPIO Pads

Bit number					7	6	5	4	3	2	1	0
ID								E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	R	GPIO0STATUS			gpioMode[0] inside [0:4] : GPIO[0] Input gpioMode[0] inside [5:9] : GPIO[0] Outnput else 0							
			LOW	0	Input Low							
			HIGH	1	Input High							
B	R	GPIO1STATUS			gpioMode[1] inside [0:4] : GPIO[1] Input gpioMode[1] inside [5:9] : GPIO[1] Outnput else 0							
			LOW	0	Input Low							
			HIGH	1	Input High							
C	R	GPIO2STATUS			gpioMode[2] inside [0:4] : GPIO[2] Input gpioMode[2] inside [5:9] : GPIO[2] Outnput else 0							
			LOW	0	Input Low							
			HIGH	1	Input High							
D	R	GPIO3STATUS			gpioMode[3] inside [0:4] : GPIO[3] Input gpioMode[3] inside [5:9] : GPIO[3] Outnput else 0							
			LOW	0	Input Low							
			HIGH	1	Input High							
E	R	GPIO4STATUS			gpioMode[4] inside [0:4] : GPIO[4] Input gpioMode[4] inside [5:9] : GPIO[4] Outnput else 0							
			LOW	0	Input Low							
			HIGH	1	Input High							

7 System features

7.1 System monitor

The chip includes a 10-bit ADC, which can be used in the following ways.

- Single-shot measurements
- Automatic measurements
- Timed measurements

Measurement request priority

When multiple measurement requests happen at the same time, the priority is as follows:

1. VBAT
2. Battery temperature
3. Battery current
4. Die temperature
5. VSYS
6. VBUS

If a measurement has been requested but the measurement has not started, a higher priority can be requested.

In the case where a low priority measurement has been requested and the system has started the measurement, a higher priority can be requested. The system will complete the lower priority measurement before the higher priority measurement.

7.1.1 Single-shot measurement

Single-shot measurements can be triggered for the following values:

- Battery temperature – using TASKNTCMEASURE on page 79
- Battery voltage, single/burst mode – using tasksTASKVBATMEASURE on page 79 and ADCCONFIG on page 81
- VSYS voltage – using task TASKVSYSMEASURE on page 80
- Battery current – using , which occurs after VBAT measurement
- VBUS voltage – using task TASKVBUS7MEASURE on page 80
- Die temperature – using task TASKTEMPMEASURE on page 80

A VBAT measurement triggered in Burst mode performs four consecutive measurements with each result available separately. Conversions are run back-to-back and completes in t_{CONV}.

Note: If a measurement must be repeated, it must be requested once the previous request is complete. Repeat measurement requests made while the previous conversion is still ongoing, are lost. Alternate measurements can be requested and are queued. See Priority for more information.

7.1.2 Automatic measurements

Automatic measurements for battery voltage are enabled in register ADCCONFIG on page 81. The default interval is 1024 ms.

7.1.2.1 Automatic measurements during charging

Battery temperature and die temperature are measured automatically at regular intervals when the battery is charging. The host software can read this value and returns the latest measurement.

The measurement intervals are as follows:

- Battery temperature – once every 64, 128, or 1024 ms. This information is used by the charging FSM.
- Die temperature – once every 4 ms, see Charger thermal regulation on page 27.

Note: To enable automatic thermistor and die temperature monitoring, set register TASKAUTOTIMUPDATE on page 82. This should also be set after changing the automated period.

7.1.3 Timed measurements

Timed measurements for battery voltage in single/Burst mode are initiated in register ADCDELTIMCONF on page 82. See Monitoring battery state of charge on page 78 for more information.

7.1.4 Measurement results

Results are stored in registers according to the following table. Some registers hold alternate results when that feature is requested. Host software must concatenate the LSB to the MSB of the result register to obtain the full accuracy.

Register	Results	Alt. results
ADCVBATRESULTMSB on page 82	VBAT	
ADCNTCRESULTMSB on page 83	Battery temperature	
ADCTEMPRESULTMSB on page 83	Die temperature	
ADCVSYSRESULTMSB on page 83	Single-shot VSYS	
ADCGP0RESULTLSBS on page 83	Lsbs for the above	
ADCVBAT0RESULTMSB on page 83	Burst VBAT 0	
ADCVBAT1RESULTMSB on page 84	Burst VBAT 1	
ADCVBAT2RESULTMSB on page 84	Burst VBAT 2	
ADCVBAT3RESULTMSB on page 84	Burst VBAT 3	Single-shot VBUS
ADCGP1RESULTLSBS on page 84	Lsbs for the above	

Table 26: ADC results in registers

The following equations can be used to interpret the results.

$$VBAT = \frac{code}{1023} VFS\_VBAT$$

Figure 7: Equation for VBAT

$$VBUS = \frac{code}{1023} VFS\_VBUS$$

Figure 8: Equation for VBUS

$$VSYS = \frac{code}{1023} VFS\_VSYS$$

Figure 9: Equation for VSYS

$$T = \frac{1}{\frac{1}{T_0} - \frac{1}{\beta} . Ln\left(\frac{2^N}{code} - 1\right)}$$

Figure 10: Battery temperature (Kelvin)

N=10 and T_0 = 298.15 K

$$T = 394.67 - 0.7926 \cdot code$$

Figure 11: Die temperature (Celcius)

$$R_M = \frac{R_B}{\frac{2^N}{code} - 1}$$

Figure 12: Equation for resistance (battery NTC)

N=10 and R_B is the bias resistor configured in ADCNTCRSEL on page 81

7.1.5 Events and interrupts

An event register and interrupt are available for each measurement and are issued once the measurement has been completed.

See registers EVENTSADCSET on page 101, EVENTSADCCLR on page 101, INTENEVENTSADCSET on page 102, and INTENEVENTSADCCLR on page 103.

7.1.6 Measuring battery temperature

Before using a battery temperature measurement, the appropriate NTC thermistor must be configured. See Battery temperature monitoring on page 25 for information about suitable thermistors and how to configure.

7.1.7 Monitoring battery state of charge

A fuel gauge algorithm run by the host allows the battery state of charge to be determined. The host periodically requests measurements from the ADC and updates the algorithm parameters

The host has the fuel gauge algorithm and periodically requests measurements from the ADC. These measurements update the algorithm parameters and allow the state of charge to be determined.

The algorithm must be provided with the battery model parameters for accurate fuel gauging. The battery model parameters can be created from the nPM PowerUP application.

Once the battery is modeled over the operating temperature range, the fuel gauge algorithm is optimized to operate over the full range of battery voltages, temperatures, and application currents.

7.1.8 Electrical specification

Symbol	Description	Min.	Typ.	Max.	Unit
VFS_VBAT	Full scale voltage for VBAT measurement		5.0		V
$V_{BATACCUR}$	Accuracy of the VBAT measurement (3 V <VBAT < 4.5V)	-1		+1	%
VFS_VBUS	Full scale voltage for VBUS measurement		7.5		V
$V_{BUSACCUR}$	Accuracy of the VBUS measurement		1.5		%
VFS_VSYS	Full scale voltage for VSYS measurement		6.375		V
$V_{SYSACCUR}$	Accuracy of the VSYS measurement		1.5		%
R_{BATNTC}	Battery temperature thermistor resistance range	2.83		1441	kΩ
C_{BATNTC}	Capacitance in parallel with the thermistor	0		100	pF
VFS_TEMP	Full scale for battery and die temperature measurements		1.5		V
t_{CONV}	Conversion time		250		µs
DNL	Differential non-linearity		<0.5		LSB
$I_{ADCAUTO}$	Current consumption, automatic measurements active		t.b.a.		µA
I_{ADCDIE}	Current consumption during die temperature measurement		t.b.a.		µA

Table 27: SAADC electrical specification

7.1.9 Electrical characteristics

The following graphs show ADC's electrical characteristics.

7.1.10 Registers

Instances

Instance	Base address	Description
ADC	0x00000500	SAADC registers ADC register map

Register overview

Register	Offset	Description
TASKVBATMEASURE	0x0	Task Take VBAT measurement
TASKNTCMEASURE	0x1	Task Take NTC measurement
TASKTEMPMEASURE	0x2	Task Take Die Temperature measurement
TASKVSYSMEASURE	0x3	Task Take VSYS measurement
TASKVBUS7MEASURE	0x7	Task Take VBUS 7V range measurement
TASKDELAYEDVBATMEASURE	0x8	Task Take delayed VBAT measurement
ADCCONFIG	0x9	ADC Configuration
ADCNTCRSEL	0xA	Select Battery NTC register
ADCAUTOTIMCONF	0xB	Auto measurement intervals
TASKAUTOTIMUPDATE	0xC	update toggle for NTC and Die temp AutoTime register bits
ADCDELTIMCONF	0xD	Vbat Delay timer control
ADCVBATRESULTMSB	0x11	ADC VBAT measurement result MSB
ADCNTCRESULTMSB	0x12	ADC NTC measurement result MSB
ADCTEMPRESULTMSB	0x13	ADC DIE TEMP measurement result MSB
ADCVSYSRESULTMSB	0x14	ADC VSYS measurement result MSB
ADCGP0RESULTLSBS	0x15	ADC result LSB's (Vbat, Ntc, Temp and Vsys)
ADCVBAT0RESULTMSB	0x16	ADC VBAT0 Burst measurement result MSB
ADCVBAT1RESULTMSB	0x17	ADC VBAT1 Burst measurement result MSB
ADCVBAT2RESULTMSB	0x18	ADC VBAT2 Burst measurement result MSB
ADCVBAT3RESULTMSB	0x19	ADC VBAT3 Burst or VBUS measurement result MSB
ADCGP1RESULTLSBS	0x1A	ADC result LSB's (Vbat_burst0, 1, 2 and 3)

7.1.10.1 TASKVBATMEASURE

Address offset: 0x0

Task Take VBAT measurement

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKVBATMEASURE			Start VBAT Measurement								
			NOEFFECT	0	no effect								
			TRIGGER	1	Trigger task								

7.1.10.2 TASKNTCMEASURE

Address offset: 0x1

Task Take NTC measurement

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKNTCMEASURE			Start Battery NTC thermistor Measurement								
			NOEFFECT	0	no effect								
			TRIGGER	1	Trigger task								

7.1.10.3 TASKTEMPMEASURE

Address offset: 0x2

Task Take Die Temperature measurement

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKTEMPMEASURE			Start Die Temperature Measurement								
			NOEFFECT	0	no effect								
			TRIGGER	1	Trigger task								

7.1.10.4 TASKVSYSMEASURE

Address offset: 0x3

Task Take VSYS measurement

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKVSYSMEASURE			Start VSYS Measurement								
			NOEFFECT	0	no effect								
			TRIGGER	1	Trigger task								

7.1.10.5 TASKVBUS7MEASURE

Address offset: 0x7

Task Take VBUS 7V range measurement

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKVBUS7MEASURE			Start VBUS 7Volt range Measurement								
			NOEFFECT	0	no effect								
			TRIGGER	1	Trigger task								

7.1.10.6 TASKDELAYEDVBATMEASURE

Address offset: 0x8

Task Take delayed VBAT measurement

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKDLYDVBATMEASURE			Start delayed VBAT Measurement								
			NOEFFECT	0	no effect								
			TRIGGER	1	Trigger task								

7.1.10.7 ADCCONFIG

Address offset: 0x9

ADC Configuration

Bit number						7	6	5	4	3	2	1	0
ID												B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	VBATAUTOENABLE			Enable VBAT Auto measurement every 1 Second								
			NOAUTO	0	Single measurement when triggered								
			AUTOENABLE	1	Make measurement every 1s								
B	RW	VBATBURSTENABLE			Enable VBAT Burst mode VBAT0, VBAT1, VBAt2, VBAT3								
			SINGLEMODE	0	Make a Single measurement								
			BURSTMODE	1	Make 4 consecutive measurements								

7.1.10.8 ADCNTCRSEL

Address offset: 0xA

Select Battery NTC register

Bit number						7	6	5	4	3	2	1	0
ID												A	A
Reset 0x01						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
ID	R/W	Field	Value ID	Value	Description								
A	RW	ADCNTCRSEL			Select value and TRIM to match Battery NTC resistance								
			Hi_Z	0	No thermistor								
			10K	1	NTC10K								
			47K	2	NTC47K								
			100K	3	NTC100K								

7.1.10.9 ADCAUTOTIMCONF

Address offset: 0xB

Auto measurement intervals

Bit number					7	6	5	4	3	2	1	0
ID									B	B	A	A
Reset 0x03					**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**
ID	R/W	Field	Value ID	Value	Description							
A	RW	NTCAUTOTIM			NTC thermistor measurement interval during Charging							
			4MS	0	4ms							
			64MS	1	64ms							
			128MS	2	128ms							
			1024MS	3	1024ms							
B	RW	TEMPAUTOTIM			Die Temp measurement interval during Charging							
			4MS	0	4ms							
			8MS	1	8ms							
			16MS	2	16ms							
			32MS	3	32ms							

7.1.10.10 TASKAUTOTIMUPDATE

Address offset: 0xC

update toggle for NTC and Die temp AutoTime register bits

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	W	TASKAUTOTIMUPDATE			update toggle, handshake signal to flag NtcAutoTim and TempAutoTim change							
			NOEFFECT	0	no effect							
			UPDATEAUTOTIM	1	Register new NtcAutoTim, TempAutoTim value							

7.1.10.11 ADCDELTIMCONF

Address offset: 0xD

Vbat Delay timer control

Bit number					7	6	5	4	3	2	1	0
ID					A	A	A	A	A	A	A	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	VBATDELTIM			Delayed Vbat measurement control 4ms(value 0) to 514ms(value 255) and the step size is 2ms.							

7.1.10.12 ADCVBATRESULTMSB

Address offset: 0x11

ADC VBAT measurement result MSB

Bit number					7	6	5	4	3	2	1	0
ID					A	A	A	A	A	A	A	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	R	VBATRESULTMSB			ADC VBAT measurement result upper 8-bits							

7.1.10.13 ADCNTCRESULTMSB

Address offset: 0x12

ADC NTC measurement result MSB

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	R	NTCRESULTMSB			ADC NTC thermistor Battery measurement result upper 8-bits								

7.1.10.14 ADCTEMPRESULTMSB

Address offset: 0x13

ADC DIE TEMP measurement result MSB

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	R	TEMPRESULTMSB			ADC Die Temperature measurement result upper 8-bits								

7.1.10.15 ADCVSYSRESULTMSB

Address offset: 0x14

ADC VSYS measurement result MSB

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	R	VSYSRESULTMSB			ADC VSYS measurement result upper 8-bits								

7.1.10.16 ADCGP0RESULTLSBS

Address offset: 0x15

ADC result LSB's (Vbat, Ntc, Temp and Vsys)

Bit number						7	6	5	4	3	2	1	0
ID						D	D	C	C	B	B	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	R	VBATRESULTLSB			VBAT measurement result LSBs								
B	R	NTCRESULTLSB			Battery NTC thermistor measurement result LSBs								
C	R	TEMPRESULTLSB			Die Temperature measurement result LSBs								
D	R	VSYSRESULTLSB			VSYS measurement result LSBs								

7.1.10.17 ADCVBAT0RESULTMSB

Address offset: 0x16

ADC VBAT0 Burst measurement result MSB

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	R	VBAT0RESULTMSB			ADC VBAT0 Burst measurement result upper 8-bits								

7.1.10.18 ADCVBAT1RESULTMSB

Address offset: 0x17

ADC VBAT1 Burst measurement result MSB

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	R	VBAT1RESULTMSB			ADC VBAT1 Burst measurement result upper 8-bits								

7.1.10.19 ADCVBAT2RESULTMSB

Address offset: 0x18

ADC VBAT2 Burst measurement result MSB

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	R	VBAT2RESULTMSB			ADC VBAT2 Burst measurement result upper 8-bits								

7.1.10.20 ADCVBAT3RESULTMSB

Address offset: 0x19

ADC VBAT3 Burst or VBUS measurement result MSB

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	R	VBAT3RESULTMSB			If TASK_VBAT_MEASURE is triggered in BURST mode, this register will contain ADC VBAT3 Burst measurement result upper 8-bits If TASK_VBUS7_MEASURE is triggered, this register will contain VBUS measurement result upper 8-bits								

7.1.10.21 ADCGP1RESULTLSBS

Address offset: 0x1A

ADC result LSB's (Vbat_burst0, 1, 2 and 3)

Bit number						7	6	5	4	3	2	1	0
ID						D	D	C	C	B	B	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	R	VBAT0RESULTLSB			Burst VBAT0 measurement result LSBs								
B	R	VBAT1RESULTLSB			Burst VBAT1 measurement result LSBs								
C	R	VBAT2RESULTLSB			Burst VBAT2 measurement result LSBs								
D	R	VBAT3RESULTLSB			Burst VBAT3 measurement result LSBs								

7.2 POF — Power-fail comparator

The power-fail comparator (POF) provides the host with an early warning of an impending power supply failure.

The POF signals the application when the supply voltage drops below a configured threshold. The POF does not reset the system, but gives the CPU time to prepare for an orderly power-down.

VSYSCOMP is an always active comparator monitoring the voltage on the **VINT** pin. It can be configured to give a warning through a GPIO to the host when VSYS drops below the threshold $VSYS_{POF}$. See register POFCONFIG on page 87.

> **Note:** Before setting $VSYS_{POF}$, VSYS must be higher than the selected threshold or it triggers a POF and resets the device. $VSYS_{POF}$ must be set to a higher voltage than the battery undervoltage protection level to avoid triggering the protection circuit.

A warning is issued in the following cases:

- VBUS is removed while the battery is empty or not connected (VBAT < $VSYS_{POF}$)
- VBUS rises above $VBUS_{OVP}$ while the battery is empty or not connected (VBAT < $VSYS_{POF}$)
- The battery is removed when VBUS is not connected
- The battery discharges until VBAT < $VSYS_{POF}$ and VBUS is not connected
- Battery voltage drops momentarily below $VSYS_{POF}$ and VBUS is not connected

When VSYS voltage falls below $VSYS_{POF}$, BUCK and LDO are disabled. BUCK output is not actively discharged until the device enters PWR_DWN_DISCHARGE.

If VSYS voltage drops, but either VBAT or VBUS remain above the respective BOR threshold, VSYS is disabled after $t_{POFWAIT}$ and registers are reset after PWR_DWN_DISCHARGE. If VSYS > VSYSCOMP, the chip powers up after t_{PWRDN} (see Power fail warning on page 86).

> **Note:** The VSYSCOMP threshold is also reset to the default setting. When VBAT > VSYSCOMP, BUCK may start up again depending on VSET[n] pins.

If power is removed, where both VBAT and VBUS drop below the respective BOR thresholds, a POF warning is given through a GPIO pin. See Power removal on page 86.

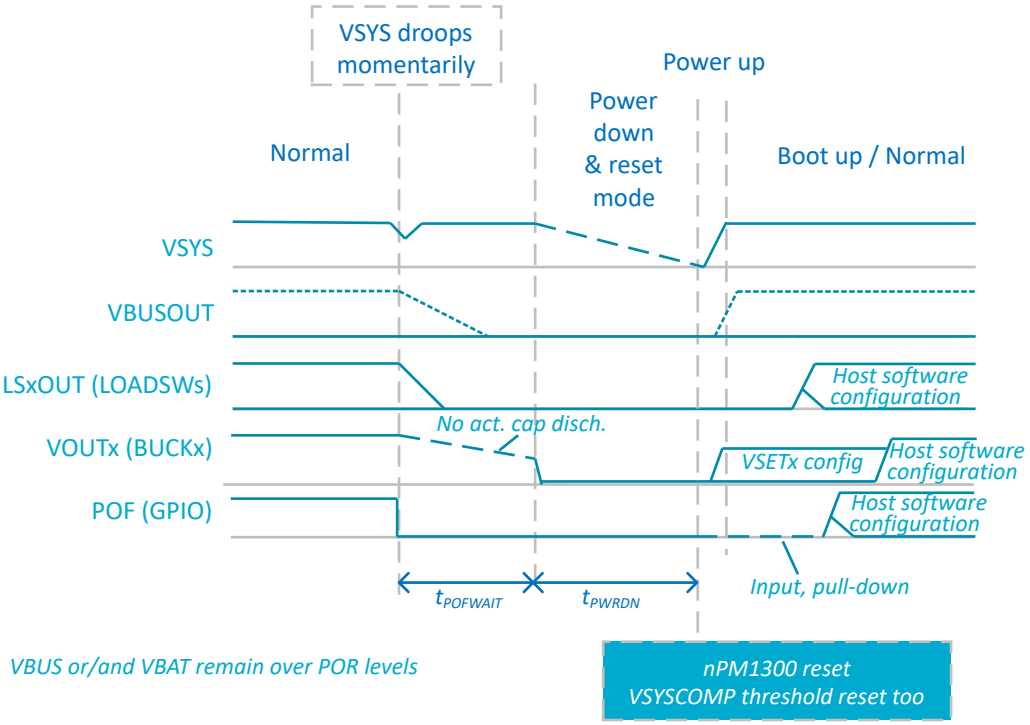

Figure 13: Power fail warning

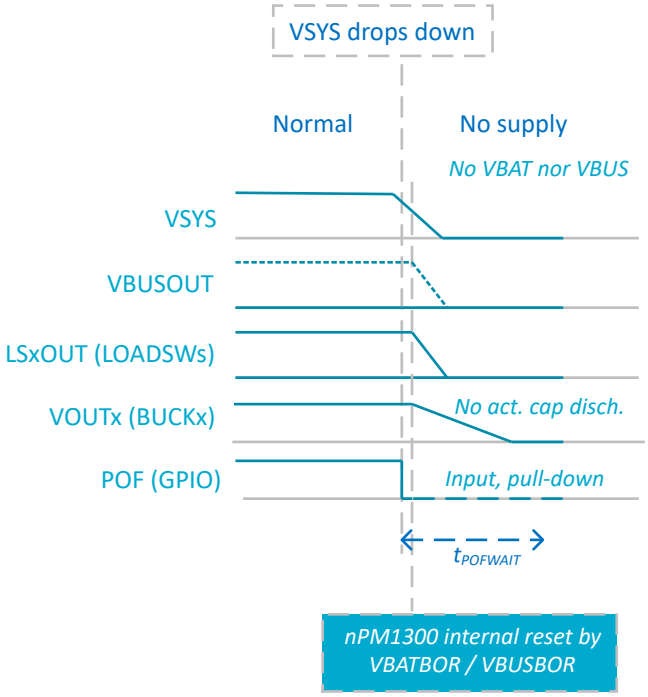

Figure 14: Power removal

To use the POF feature, set POFWARNPOLARITY and POFENA to `1` in register POFCONFIG on page 87. GPIO settings are located in GPIO — General purpose input/output on page 62. When setting GPIOs to output, the host software should disable any pull up or pull down on that GPIO, as the default is for the pull down to be enabled after reset.

7.2.1 Electrical specification

Symbol	Description	Min.	Typ.	Max.	Unit
VSYSCOMP	VSYSCOMP rising threshold, default (Note)		2.9		V
$VSYS_{POF}$	VSYSCOMP falling threshold		2.6 2.7 2.8 (default) 2.9 3.0 3.1 3.2 3.3 3.4 3.5		V
t_{POF}	Reaction time (from crossing the threshold to edge on the warning signal)		1		ms
t_{PWRDN}	Time in Power-down mode		100		ms
$t_{POFWAIT}$	Time delay before activating active output capacitor discharge and disconnecting VBAT and VBUS from VSYS		30		ms

Table 28: POF electrical specification

Note: The rising threshold is always 100 mV (typ.) above the falling threshold.

7.2.2 Registers

Instances

Instance	Base address	Description
POF	0x00000900	POF Registers POF register map

Register overview

Register	Offset	Description
POFCONFIG	0x0	Power Failure Detection block configuration

7.2.2.1 POFCONFIG

Address offset: 0x0

Power Failure Detection block configuration

Bit number						7	6	5	4	3	2	1	0
ID								C	C	C	C	B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	POFENA			Enable Power Failure feature								
			OFF	0	Off								
			ENABLED	1	WarningEnabled								
B	RW	POFWARNPOLARITY			Power Failure Warning polarity								
			LOACTIVE	0	LoActive								
			HIACTIVE	1	HiActive								
C	RW	POFVSYSTHRESHSEL			Vsys Comparator Threshold Select								
			2V8	0	2.8V								
			2V6	1	2.6V								
			2V7	2	2.7V								
			2V9	3	2.9V								
			3V0	4	3.0V								
			3V1	5	3.1V								
			3V2	6	3.2V								
			3V3	7	3.3V								
			3V4	8	3.4V								
			3V5	9	3.5V								
			unused10	10	set to 2.8V								
			unused11	11	set to 2.8V								
			unused12	12	set to 2.8V								
			unused13	13	set to 2.8V								
			unused14	14	set to 2.8V								
			unused15	15	set to 2.8V								

7.3 TIMER — Timer/monitor

TIMER can be used in different ways, depending on configuration.

- General purpose timer
- Watchdog timer
- Wake-up timer
- Boot monitor

TIMER is a 24-bit timer running at the frequency of the timer clock, f_{TIMER}, and has a prescaler.

TIMER only runs one timer at a time because it is shared for all functions. The wake-up timer is intended for use during Hibernate mode to wake the system at a programmable interval. The watchdog timer and general purpose timer are to be used when the system is not in ship or hibernate mode.

TIMER is controlled by register TIMERCONFIG on page 92. The start value is configured with TIMERHIBYTE on page 93, TIMERMIDBYTE on page 93, and TIMERLOBYTE on page 94. The settings are applied with TIMERTARGETSTROBE on page 92. TIMER is started with TIMERSET on page 91 and is stopped with TIMERCLR on page 92

7.3.1 Boot monitor

Boot monitor is the timer default after power up. It makes sure that the host boots up successfully.

If bit TASK.TIMER.DIS in register TIMERCLR on page 92 is not set within t_{BOOT}, a power cycle occurs.

Host software can disable the boot monitor to prevent interference with firmware updates. When bit BOOT.TIMER.EN in register SCRATCH0 on page 122 is set, the boot monitor remains enabled

even if the chip is reset, except if it's a power-on reset. Removing both VBAT and VBUS, or clearing the BOOT.TIMER.EN bit, deactivates the timer during the next power-up.

7.3.2 Watchdog timer

Watchdog timer expiration can be configured by host software to generate an NRESETOUT through a GPIO or a power cycle.

Power cycle means internally disconnecting VINT from the VBAT and VBUS power path. BUCK[n] and LOADSW[n] are actively pulled low for 100 ms. The device is reset and BUCK[n] re-enabled. Active pull-downs are present at pin **VOUT1**, **VOUT2**, **LSOUT1**, and **L2OUT2** during t_{PWRDN}.

The watchdog timer can issue a pre-warning interrupt, $t_{PREWARN}$, before expiration. The reset pulse (active low) through the NRESETOUT GPIO lasts for t_{RESET}. Watchdog can be pushed out using register WATCHDOGKICK on page 92.

The pre-warning interrupt is generated one cycle of the selected prescaler before expiry of the watchdog occurs.

The following figures show a watchdog reset and a power cycle.

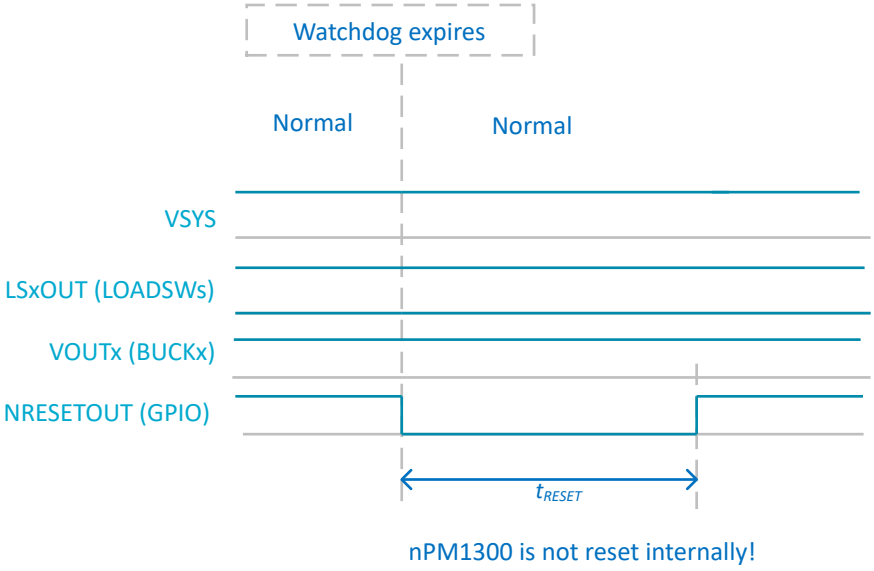

Figure 15: Watchdog reset

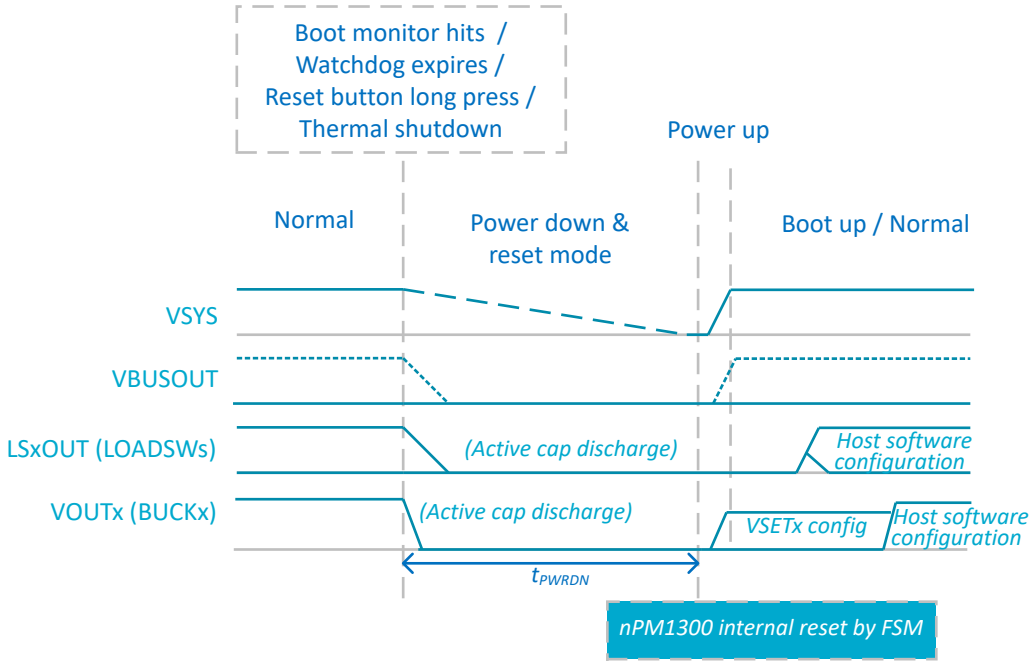

Figure 16: Power cycle

Note: For the thermal shutdown case, t_{PWRDN} will be longer as it waits for the die temperature to cool down below TSD - TSD_{HYST}.

7.3.3 Wake-up timer

The wake-up timer wakes the system from Hibernate mode.

Host software configures the timer before the device enters Hibernate mode, see Ship and Hibernate modes on page 94.

7.3.4 General purpose timer

The general purpose timer interrupts the host after a timeout with WATCHDOGWARNING.

Prescaler is configured in register TIMERCONFIG on page 92 with the default set to 16 ms.

When the prescaler is configured to 16 ms in TIMERCONFIG on page 92 and TIMERHIBYTE on page 93 is 5, TIMERMIDBYTE on page 93 is 2 and TIMERLOBYTE on page 94 is 1, then the general purpose timer will wake after 5251 seconds.

7.3.5 Electrical specification

Both prescaler settings (2 ms and 16 ms) are included. Values in parenthesis are for the 2 ms prescaler.

Symbol	Description	Min.	Typ.	Max.	Unit
f_{TIMER}	Frequency of timer clock		64 (512)		Hz
$t_{PREWARN}$	Time between watchdog timer interrupt and reset/power cycle		16 (2)		ms
t_{PER_MIN}	Minimum time period		16 (2)		ms
t_{PER_MAX}	Maximum time period		3 (9)		days (hours)
t_{BOOT}	Time after which a power cycle is done in case no traffic is seen on TWI		10		s
t_{PWRDN}	Length of power cycle		100		ms
t_{RESET}	Length of reset pulse		100		ms
f_{ACCUR}	Accuracy of timer clock	t.b.a.		t.b.a.	%
t_{ACCUR}	Accuracy of time period	t.b.a.		t.b.a.	

Table 29: TIMER electrical specification

7.3.6 Registers

Instances

Instance	Base address	Description
TIMER	0x00000700	TIMER Registers TIMER register map

Register overview

Register	Offset	Description
TIMERSET	0x0	Start Timer
TIMERCLR	0x1	Stop Timer
TIMERTARGETSTROBE	0x3	Strobe for timer Target
WATCHDOGKICK	0x4	Watchdog kick
TIMERCONFIG	0x5	Timer mode selection
TIMERSTATUS	0x6	Timers Status
TIMERHIBYTE	0x8	Timer Most Significant Byte
TIMERMIDBYTE	0x9	Timer Middle Byte
TIMERLOBYTE	0xA	Timer Least Significant Byte

7.3.6.1 TIMERSET

Address offset: 0x0

Start Timer

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKTIMEREN			Start Timer								
			NOEFFECT	0	no effect								
			SET	1	Timer Start request								

7.3.6.2 TIMERCLR

Address offset: 0x1

Stop Timer

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKTIMERDIS			Stop Timer								
			NOEFFECT	0	no effect								
			SET	1	Timer Stop request								

7.3.6.3 TIMERTARGETSTROBE

Address offset: 0x3

Strobe for timer Target

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKTIMERTARGETSTROBE			Timer target strobe								
			NOEFFECT	0	no effect								
			SET	1	load timer target (24 bit timer val)								

7.3.6.4 WATCHDOGKICK

Address offset: 0x4

Watchdog kick

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKWATCHDOGKICK			Watchdog kick								
			NOEFFECT	0	no effect								
			Kick	1	kick watchdog								

7.3.6.5 TIMERCONFIG

Address offset: 0x5

Timer mode selection

Bit number						7	6	5	4	3	2	1	0
ID										B	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	TIMERMODESEL			Select Watchdog and timer modes								
			BOOTMONITOR	0	Boot Monitor								
			WATCHDOGWARNING	1	Watchdog Warning								
			WATCHDOGRESET	2	Watchdog Reset								
			GENPURPOSETIMER	3	GenPurpose Timer								
			WAKEUPTIMER	4	Wakeup Timer								
B	RW	TIMERPRESCALER			Switches between 16ms and 2ms Timer Prescale								
			SLOW	0	16ms Prescale								
			FAST	1	2ms Prescale								

7.3.6.6 TIMERSTATUS

Address offset: 0x6

Timers Status

Bit number						7	6	5	4	3	2	1	0
ID												B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	R	BOOTMONITORACTIVE			BootMonitor Active								
			INACTIVE	0	Boot Monitor not running								
			ACTIVE	1	BootMonitor running								
B	R	SLOWDOMAINCONF			slowDomain Configured								
			NOTCONFIG	0	No config, TASK_RESET_CFG clears.								
			CONFIG	1	At least one timer related Strobe has been active to configure slowDomain								

7.3.6.7 TIMERHIBYTE

Address offset: 0x8

Timer Most Significant Byte

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	TIMERHIBYTE			Timer Most Significant Byte of 3								

7.3.6.8 TIMERMIDBYTE

Address offset: 0x9

Timer Middle Byte

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	TIMERMIDBYTE			Timer Middle Byte of 3								

7.3.6.9 TIMERLOBYTE

Address offset: 0xA

Timer Least Significant Byte

Bit number									7	6	5	4	3	2	1	0
ID									A	A	A	A	A	A	A	A
Reset 0x00									**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field			Value ID		Value		Description							
A	RW	TIMERLOBYTE							Timer Least Significant Byte of 3							

7.4 Ship and Hibernate modes

Ship and Hibernate modes isolate the battery from the system and minimize the quiescent current.

Hibernate mode is identical to Ship mode with the exception that, in hibernate mode, the timer is running and functions as an additional wake-up source.

The device enters Ship mode through register TASKENTERSHIPMODE on page 95. Register SHPHLDCONFIG on page 96 configures the button press time, and register TASKSHPHLDCFGSTROBE on page 95 applies the configured value. When VBUS is not present, the device enters Ship mode immediately. The host software waits until VBUS is disconnected and discharged before writing to the register.

The device enters Hibernate mode through register TASKENTERHIBERNATE on page 95. To apply the timer value, registers TIMERHIBYTE on page 93, TIMERMIDBYTE on page 93, and TIMERLOBYTE on page 94 must be configured before register TIMERTARGETSTROBE on page 92. In Hibernate mode, the quiescent current is higher compared to Ship mode because the low-power timer is running.

Exiting Hibernate mode using a button press must be configured in register SHPHLDCONFIG on page 96 and TASKSHPHLDCFGSTROBE on page 95.

When entering Ship mode, BUCK can be configured to discharge by enabling their pull downs, see BUCKCTRL0 on page 53.

> **Note:** SHPHLDCONFIG on page 96 and TASKSHPHLDCFGSTROBE on page 95 must be set before entering either Ship or Hibernate modes.

The following are alternative ways to exit Ship and Hibernate modes.

- Pulling pin SHPHLD low for a minimum period of $t_{shipToActive}$ (see SHPHLDCONFIG on page 96). A push button to GND is required.
- Applying a voltage on VBUS > $VBUS_{POR}$.
- Exiting automatically through the Wake-up timer (only from Hibernate mode).

7.4.1 Registers

Instances

Instance	Base address	Description
SHIP	0x00000B00	SHIP Registers SHPHLD register map

Register overview

Register	Offset	Description
TASKENTERHIBERNATE	0x0	Task Enter Hibernate
TASKSHPHLDCFGSTROBE	0x1	Task Ship Hold config
TASKENTERSHIPMODE	0x2	Task enter ShipMode
TASKRESETCFG	0x3	Request reset config
SHPHLDCONFIG	0x4	Ship Hold button press timer config
SHPHLDSTATUS	0x5	Status of the SHPHLD pin
LPRESETCONFIG	0x6	Long press reset config register

7.4.1.1 TASKENTERHIBERNATE

Address offset: 0x0

Task Enter Hibernate

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKENTERHIBERNATE			Enter Hibernate (Shipmode with Wakeup Timer)								
			NOEFFECT	0	no effect								
			TRIGGER	1	trigger task								

7.4.1.2 TASKSHPHLDCFGSTROBE

Address offset: 0x1

Task Ship Hold config

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKSHPHLDCONFIGSTROBE			Load the SHPHLD Config								
			NOEFFECT	0	no effect								
			TRIGGER	1	strobe config								

7.4.1.3 TASKENTERSHIPMODE

Address offset: 0x2

Task enter ShipMode

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKENTERSHIPMODE			Enter Shipmode (without Wakeup timer)								
			NOEFFECT	0	no effect								
			TRIGGER	1	trigger task								

7.4.1.4 TASKRESETCFG

Address offset: 0x3

Request reset config

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKSHPHLDRSTCONFIG			Use to reset config settings								
			NOEFFECT	0	no effect								
			TRIGGER	1	reset								

7.4.1.5 SHPHLDCONFIG

Address offset: 0x4

Ship Hold button press timer config

Bit number						7	6	5	4	3	2	1	0
ID										B	A	A	A
Reset 0x03						**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**
ID	R/W	Field	Value ID	Value	Description								
A	RW	SHPHLDTIM			Ship-Hold press timer								
			16ms	0	16ms								
			32ms	1	32ms								
			64ms	2	64ms								
			96ms	3	96ms (default)								
			304ms	4	304ms								
			608ms	5	608ms								
			1008ms	6	1008ms								
			3008ms	7	3008ms								
B	RW	SHPHLDPOLARITY			Polarity of shphld								
			NOEFFECT	0	no effect								
			INVERT	1	shphld inverted								

7.4.1.6 SHPHLDSTATUS

Address offset: 0x5

Status of the SHPHLD pin

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	R	SHPHLDPINSTATUS			Ship Hold pin Status								
			LOW	0	Low								
			HIGH	1	High								

7.4.1.7 LPRESETCONFIG

Address offset: 0x6

Long press reset config register

Bit number						7	6	5	4	3	2	1	0
ID												B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	LONGTIMRESETDIS			Long press 10s timer enable								
			ENABLED	0	LongPress Enabled								
			DISABLED	1	Disabled								
B	RW	LONGTIMTWOBUTTO			Select one (default) or two buttons to perform longpress reset								
			SHPHLD	0	SHPHLD								
			SHPHLDGPIO0	1	SHPHLD GPIO0								

7.4.2 Electrical specification

Symbol	Description	Min.	Typ.	Max.	Unit
$t_{shipToActive}$	Duration **SHPHLD** pin must be held low to exit Ship or Hibernate mode		16 32 64 96 (default) 304 608 1008 3008		ms
$t_{RESETBUT}$	Time duration for button press to cause a power cycle		10		s
R_{SHPHLD}	Pull-up resistor on **SHPHLD** pin		50		kΩ

Table 30: Ship mode electrical specification

7.5 RESET — Reset control

The **SHPHLD** pin is a reset control, in addition to being used for exiting Ship and Hibernate mode.

The **SHPHLD** pin has an internal pull-up resistor R_{SHPHLD} to VBAT. The functionality of the pin is determined by the device mode.

Normal mode

If configured, a short press of the button sends an interrupt to the host. Host software reads the pin state in register SHPHLDSTATUS on page 96.

A long press (> $t_{RESETBUT}$) of the button causes a power cycle and resets the whole system. This feature is enabled by default after power-up, but can be disabled by the host software, see LPRESETCONFIG on page 96.

In ship and hibernate modes

Pressing the button for longer than $t_{shipToActive}$ wakes up the device from Ship or Hibernate mode, performs an internal reset, and transitions to normal mode.

Two-button reset

A two-button reset is implemented by connecting one button to the **SHPHLD** pin and another button to GPIO0. This feature must be enabled by host software in LPRESETCONFIG on page 96. Pressing both buttons for longer than $t_{RESETBUT}$ causes a power cycle.

Host software reset

Host software can reset the device by writing the TASKSWRESET bit in register TASKSWRESET on page 100. As a consequence, a power cycle is performed. A reset is not possible in Ship or Hibernate mode.

Scratch registers, reason for reset

Two context registers are available: SCRATCH0 on page 122 and SCRATCH1 on page 122. Only POR and TASKCLRERRLOG initializes these registers. Register RSTCAUSE on page 123 contains the reason for the first reset encountered.

7.6 TWI — I²C compatible two-wire interface

TWI is a two-wire interface that controls and monitors the device state through registers.

Main Features

- I²C compatible up to 400 kHz
- TWI clock supports 100 kHz to 1 MHz

A GPIO pin can be set as an interrupt pin, see GPIO — General purpose input/output on page 62.

Interface supply

TWI is supplied by VDDIO. It is recommended to connect **VDDIO** to a BUCK output, **VOUT1**, or **VOUT2**. VDDIO must be present in all operating modes of the chip, except in Ship and Hibernate modes.

Addressing

The 7-bit slave address is 110 1011.

The registers have 16-bit addressing and 8-bit data. The upper address byte is the register instance base address (bank address). The lower byte is the offset within an instance (bank).

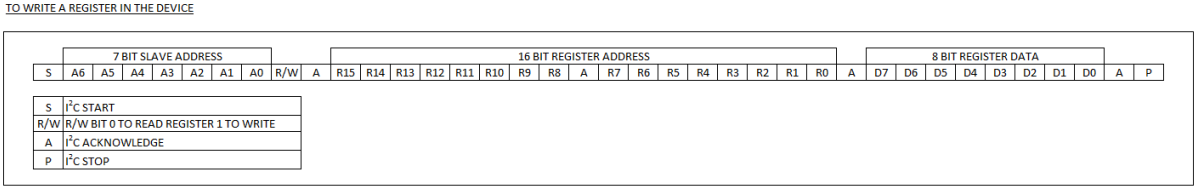

Figure 17: TWI write example

7.6.1 TWI electrical specification

Symbol	Description	Min.	Typ.	Max.	Units
F_{SCL}	SCL clock frequency	100		1000	kbps
TSU_{DAT}	Data setup time before positive edge on SCL, all modes	t.b.a.			ns
THD_{DAT}	Data hold time after negative edge on SCL, all modes	t.b.a.			ns
THD_{STA_100K}	Hold time from for START condition (SDA low to SCL low), 100 kbps	t.b.a.			ns
THD_{STA_400K}	Hold time from for START condition (SDA low to SCL low), 400 kbps	t.b.a.			ns
THD_{STA_1M}	Hold time from for START condition (SDA low to SCL low), 1 Mbps	t.b.a.			ns
TSU_{STO_100K}	Setup time from SCL high to STOP condition, 100 kbps	t.b.a.			ns
TSU_{STO_400K}	Setup time from SCL high to STOP condition, 400 kbps	t.b.a.			ns
TSU_{STO_1M}	Setup time from SCL high to STOP condition, 1 Mbps	t.b.a.			ns
$TBUF_{100K}$	Bus free time between STOP and START conditions, 100 kbps		t.b.a.		ns
$TBUF_{400K}$	Bus free time between STOP and START conditions, 400 kbps		t.b.a.		ns
$TBUF_{1M}$	Bus free time between STOP and START conditions, 1 Mbps		t.b.a.		ns

Table 31: TWI electrical specification

7.6.1.1 TWI timing diagram

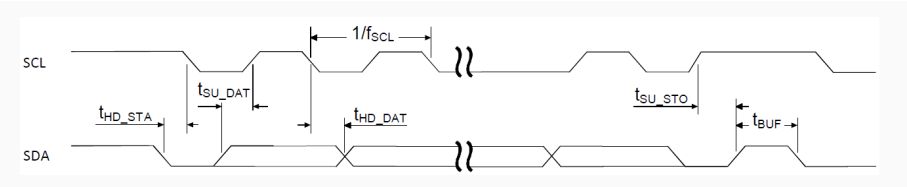

Figure 18: TWI timing diagram

7.7 Event and interrupt registers

This section details the event and interrupt related registers.

7.7.1 Registers

Instances

Instance	Base address	Description
MAIN	0x00000000	MAIN Registers MAIN Register map

Register overview

Register	Offset	Description
TASKSWRESET	0x1	Task Force a full reboot power-cycle
EVENTSADCSET	0x2	ADC Events Event Set
EVENTSADCCLR	0x3	ADC Events Event Clear
INTENEVENTSADCSET	0x4	ADC Events Interrupt Enable Set
INTENEVENTSADCCLR	0x5	ADC Events Interrupt Enable Clear
EVENTSBCHARGER0SET	0x6	Battery Charger Temperature Events Event Set
EVENTSBCHARGER0CLR	0x7	Battery Charger Temperature Events Event Clear
INTENEVENTSBCHARGER0SET	0x8	Battery Charger Temperature Events Interrupt Enable Set
INTENEVENTSBCHARGER0CLR	0x9	Battery Charger Temperature Events Interrupt Enable Clear
EVENTSBCHARGER1SET	0xA	Battery Charger Status Events Event Set
EVENTSBCHARGER1CLR	0xB	Battery Charger Status Events Event Clear
INTENEVENTSBCHARGER1SET	0xC	Battery Charger Status Events Interrupt Enable Set
INTENEVENTSBCHARGER1CLR	0xD	Battery Charger Status Events Interrupt Enable Clear
EVENTSBCHARGER2SET	0xE	Battery Charger Battery Events Event Set
EVENTSBCHARGER2CLR	0xF	Battery Charger Battery Events Event Clear
INTENEVENTSBCHARGER2SET	0x10	Battery Charger Battery Events Interrupt Enable Set
INTENEVENTSBCHARGER2CLR	0x11	Battery Charger Battery Events Interrupt Enable Clear
EVENTSSHPHLDSET	0x12	ShipHold pin Events Event Set
EVENTSSHPHLDCLR	0x13	ShipHold pin Events Event Clear
INTENEVENTSSHPHLDSET	0x14	ShipHold pin Events Interrupt Enable Set
INTENEVENTSSHPHLDCLR	0x15	ShipHold pin Events Interrupt Enable Clear
EVENTSVBUSIN0SET	0x16	VBUSIN Voltage Detection Events Event Set
EVENTSVBUSIN0CLR	0x17	VBUSIN Voltage Detection Events Event Clear
INTENEVENTSVBUSIN0SET	0x18	VBUSIN Voltage Detection Events Interrupt Enable Set
INTENEVENTSVBUSIN0CLR	0x19	VBUSIN Voltage Detection Events Interrupt Enable Clear
EVENTSVBUSIN1SET	0x1A	VBUSIN Thermal and USB Events Event Set
EVENTSVBUSIN1CLR	0x1B	VBUSIN Thermal and USB Events Event Clear
INTENEVENTSVBUSIN1SET	0x1C	VBUSIN Thermal and USB Events Interrupt Enable Set
INTENEVENTSVBUSIN1CLR	0x1D	VBUSIN Thermal and USB Events Interrupt Enable Clear
EVENTSGPIOSET	0x22	GPIO Event Event Set
EVENTSGPIOCLR	0x23	GPIO Event Event Clear
INTENEVENTSGPIOSET	0x24	GPIO Event Interrupt Enable Set
INTENEVENTSGPIOCLR	0x25	GPIO Event Interrupt Enable Clear

7.7.1.1 TASKSWRESET

Address offset: 0x1

Task Force a full reboot power-cycle

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	W	TASKSWRESET			Turn off all Supplies and apply internal reset							
			NOEFFECT	0	no effect							
			TRIGGER	1	Trigger task							

7.7.1.2 EVENTSADCSET

Address offset: 0x2

ADC Events Event Set

Bit number					7	6	5	4	3	2	1	0
ID					H	G	F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1S	EVENTADCVBATRDY			VBAT measurement finished. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							
B	RW W1S	EVENTADCNTCRDY			Battery NTC measurement finished. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							
C	RW W1S	EVENTADCTEMPRDY			Internal Die Temperature measurement finished. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							
D	RW W1S	EVENTADCVSYSRDY			VSYS Voltage measurement measurement finished. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							
E	RW W1S	EVENTADCVSET1RDY			DCDC VSET1 pin measurement finished. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							
F	RW W1S	EVENTADCVSET2RDY			DCDC VSET2 pin measurement finished. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							
G	RW W1S	EVENTADCIBATRDY			IBAT measurement finished. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							
H	RW W1S	EVENTADCVBUS7V0F			VBUS (7Volt range) measurement finished. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							

7.7.1.3 EVENTSADCCLR

Address offset: 0x3

ADC Events Event Clear

Bit number						7	6	5	4	3	2	1	0
ID						H	G	F	E	D	C	B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW W1C	EVENTADCVBATRDY			VBAT measurement finished. Writing 1 clears the event (e.g. to acknowledge an interrupt).								
			LOW	0	low								
			HIGH	1	high								
B	RW W1C	EVENTADCNTCRDY			Battery NTC measurement finished. Writing 1 clears the event (e.g. to acknowledge an interrupt).								
			LOW	0	low								
			HIGH	1	high								
C	RW W1C	EVENTADCTEMPRDY			Internal Die Temperature measurement finished. Writing 1 clears the event (e.g. to acknowledge an interrupt).								
			LOW	0	low								
			HIGH	1	high								
D	RW W1C	EVENTADCVSYSRDY			VSYS Voltage measurement measurement finished. Writing 1 clears the event (e.g. to acknowledge an interrupt).								
			LOW	0	low								
			HIGH	1	high								
E	RW W1C	EVENTADCVSET1RDY			DCDC VSET1 pin measurement finished. Writing 1 clears the event (e.g. to acknowledge an interrupt).								
			LOW	0	low								
			HIGH	1	high								
F	RW W1C	EVENTADCVSET2RDY			DCDC VSET2 pin measurement finished. Writing 1 clears the event (e.g. to acknowledge an interrupt).								
			LOW	0	low								
			HIGH	1	high								
G	RW W1C	EVENTADCIBATRDY			IBAT measurement finished. Writing 1 clears the event (e.g. to acknowledge an interrupt).								
			LOW	0	low								
			HIGH	1	high								
H	RW W1C	EVENTADCVBUS7V0F			VBUS (7Volt range) measurement finished. Writing 1 clears the event (e.g. to acknowledge an interrupt).								
			LOW	0	low								
			HIGH	1	high								

7.7.1.4 INTENEVENTSADCSET

Address offset: 0x4

ADC Events Interrupt Enable Set

Bit number						7	6	5	4	3	2	1	0
ID						H	G	F	E	D	C	B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW W1S	EVENTADCVBATRDY			Writing 1 enables interrupts from EVENTADCVBATRDY								
			LOW	0	low								
			HIGH	1	high								

Bit number					7	6	5	4	3	2	1	0
ID					H	G	F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
B	RW W1S	EVENTADCNTCRDY			Writing 1 enables interrupts from EVENTADCNTCRDY							
			LOW	0	low							
			HIGH	1	high							
C	RW W1S	EVENTADCTEMPRDY			Writing 1 enables interrupts from EVENTADCTEMPRDY							
			LOW	0	low							
			HIGH	1	high							
D	RW W1S	EVENTADCVSYSRDY			Writing 1 enables interrupts from EVENTADCVSYSRDY							
			LOW	0	low							
			HIGH	1	high							
E	RW W1S	EVENTADCVSET1RDY			Writing 1 enables interrupts from EVENTADCVSET1RDY							
			LOW	0	low							
			HIGH	1	high							
F	RW W1S	EVENTADCVSET2RDY			Writing 1 enables interrupts from EVENTADCVSET2RDY							
			LOW	0	low							
			HIGH	1	high							
G	RW W1S	EVENTADCIBATRDY			Writing 1 enables interrupts from EVENTADCIBATRDY							
			LOW	0	low							
			HIGH	1	high							
H	RW W1S	EVENTADCVBUS7V0F			Writing 1 enables interrupts from EVENTADCVBUS7V0RDY							
			LOW	0	low							
			HIGH	1	high							

7.7.1.5 INTENEVENTSADCCLR

Address offset: 0x5

ADC Events Interrupt Enable Clear

Bit number					7	6	5	4	3	2	1	0
ID					H	G	F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1C	EVENTADCVBATRDY			Writing 1 disables interrupts from EVENTADCVBATRDY							
			LOW	0	low							
			HIGH	1	high							
B	RW W1C	EVENTADCNTCRDY			Writing 1 disables interrupts from EVENTADCNTCRDY							
			LOW	0	low							
			HIGH	1	high							
C	RW W1C	EVENTADCTEMPRDY			Writing 1 disables interrupts from EVENTADCTEMPRDY							
			LOW	0	low							

Bit number						7	6	5	4	3	2	1	0
ID						H	G	F	E	D	C	B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
			HIGH	1	high								
D	RW W1C	EVENTADCVSYSRDY			Writing 1 disables interrupts from EVENTADCVSYSRDY								
			LOW	0	low								
			HIGH	1	high								
E	RW W1C	EVENTADCVSET1RDY			Writing 1 disables interrupts from EVENTADCVSET1RDY								
			LOW	0	low								
			HIGH	1	high								
F	RW W1C	EVENTADCVSET2RDY			Writing 1 disables interrupts from EVENTADCVSET2RDY								
			LOW	0	low								
			HIGH	1	high								
G	RW W1C	EVENTADCIBATRDY			Writing 1 disables interrupts from EVENTADCIBATRDY								
			LOW	0	low								
			HIGH	1	high								
H	RW W1C	EVENTADCVBUS7V0F			Writing 1 disables interrupts from EVENTADCVBUS7V0RDY								
			LOW	0	low								
			HIGH	1	high								

7.7.1.6 EVENTSBCHARGER0SET

Address offset: 0x6

Battery Charger Temperature Events Event Set

Bit number						7	6	5	4	3	2	1	0
ID								F	E	D	C	B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW W1S	EVENTNTCCOLD			Event when Cold Battery detected from NTC measure. Writing 1 sets the event (for debugging).								
			LOW	0	low								
			HIGH	1	high								
B	RW W1S	EVENTNTCCOOL			Event when Cool Battery detected from NTC measure. Writing 1 sets the event (for debugging).								
			LOW	0	low								
			HIGH	1	high								
C	RW W1S	EVENTNTCWARM			Event when Warm Battery detected from NTC measure. Writing 1 sets the event (for debugging).								
			LOW	0	low								
			HIGH	1	high								
D	RW W1S	EVENTNTCHOT			Event when Hot Battery detected from NTC measure. Writing 1 sets the event (for debugging).								
			LOW	0	low								
			HIGH	1	high								
E	RW W1S	EVENTDIETEMPHIGH			Event when die high temperature detected from Die Temp measure. Writing 1 sets the event (for debugging).								

Bit number					7	6	5	4	3	2	1	0
ID							F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
			LOW	0	low							
			HIGH	1	high							
F	RW	EVENTDIETEMPRESU			Event when die resume temperature detected from Die Temp measure.							
	W1S				Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							

7.7.1.7 EVENTSBCHARGER0CLR

Address offset: 0x7

Battery Charger Temperature Events Event Clear

Bit number					7	6	5	4	3	2	1	0
ID							F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	EVENTNTCCOLD			Event when Cold Battery detected from NTC measure. Writing 1 clears the							
	W1C				event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							
B	RW	EVENTNTCCOOL			Event when Cool Battery detected from NTC measure. Writing 1 clears the							
	W1C				event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							
C	RW	EVENTNTCWARM			Event when Warm Battery detected from NTC measure. Writing 1 clears the							
	W1C				event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							
D	RW	EVENTNTCHOT			Event when Hot Battery detected from NTC measure. Writing 1 clears the							
	W1C				event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							
E	RW	EVENTDIETEMPHIGH			Event when die high temperature detected from Die Temp measure. Writing							
	W1C				1 clears the event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							
F	RW	EVENTDIETEMPRESU			Event when die resume temperature detected from Die Temp measure.							
	W1C				Writing 1 clears the event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							

7.7.1.8 INTENEVENTSBCHARGER0SET

Address offset: 0x8

Battery Charger Temperature Events Interrupt Enable Set

Bit number					7	6	5	4	3	2	1	0
ID							F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1S	EVENTNTCCOLD			Writing 1 enables interrupts from EVENTNTCCOLD							
			LOW	0	low							
			HIGH	1	high							
B	RW W1S	EVENTNTCCOOL			Writing 1 enables interrupts from EVENTNTCCOOL							
			LOW	0	low							
			HIGH	1	high							
C	RW W1S	EVENTNTCWARM			Writing 1 enables interrupts from EVENTNTCWARM							
			LOW	0	low							
			HIGH	1	high							
D	RW W1S	EVENTNTCHOT			Writing 1 enables interrupts from EVENTNTCHOT							
			LOW	0	low							
			HIGH	1	high							
E	RW W1S	EVENTDIETEMPHIGH			Writing 1 enables interrupts from EVENTDIETEMPHIGH							
			LOW	0	low							
			HIGH	1	high							
F	RW W1S	EVENTDIETEMPRESU			Writing 1 enables interrupts from EVENTDIETEMPRESUME							
			LOW	0	low							
			HIGH	1	high							

7.7.1.9 INTENEVENTSBCHARGER0CLR

Address offset: 0x9

Battery Charger Temperature Events Interrupt Enable Clear

Bit number					7	6	5	4	3	2	1	0
ID							F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1C	EVENTNTCCOLD			Writing 1 disables interrupts from EVENTNTCCOLD							
			LOW	0	low							
			HIGH	1	high							
B	RW W1C	EVENTNTCCOOL			Writing 1 disables interrupts from EVENTNTCCOOL							
			LOW	0	low							
			HIGH	1	high							
C	RW W1C	EVENTNTCWARM			Writing 1 disables interrupts from EVENTNTCWARM							
			LOW	0	low							
			HIGH	1	high							
D	RW W1C	EVENTNTCHOT			Writing 1 disables interrupts from EVENTNTCHOT							
			LOW	0	low							

Bit number					7	6	5	4	3	2	1	0
ID							F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
			HIGH	1	high							
E	RW W1C	EVENTDIETEMPHIGH			Writing 1 disables interrupts from EVENTDIETEMPHIGH							
			LOW	0	low							
			HIGH	1	high							
F	RW W1C	EVENTDIETEMPRESU			Writing 1 disables interrupts from EVENTDIETEMPRESUME							
			LOW	0	low							
			HIGH	1	high							

7.7.1.10 EVENTSBCHARGER1SET

Address offset: 0xA

Battery Charger Status Events Event Set

Bit number					7	6	5	4	3	2	1	0
ID							F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1S	EVENTSUPPLEMENT			Event supplement mode activated. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							
B	RW W1S	EVENTCHGTRICKLE			Event Trickle Charge started. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							
C	RW W1S	EVENTCHGCC			Event Constant Current charging started. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							
D	RW W1S	EVENTCHGCV			Event Constant Voltage charging started. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							
E	RW W1S	EVENTCHGCOMPLETED			Event charging completed (Battery Full). Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							
F	RW W1S	EVENTCHGERROR			Event charging error. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							

7.7.1.11 EVENTSBCHARGER1CLR

Address offset: 0xB

Battery Charger Status Events Event Clear

Bit number					7	6	5	4	3	2	1	0
ID						F	E	D	C	B	A	
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1C	EVENTSUPPLEMENT			Event supplement mode activated. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							
B	RW W1C	EVENTCHGTRICKLE			Event Trickle Charge started. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							
C	RW W1C	EVENTCHGCC			Event Constant Current charging started. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							
D	RW W1C	EVENTCHGCV			Event Constant Voltage charging started. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							
E	RW W1C	EVENTCHGCOMPLETED			Event charging completed (Battery Full). Writing 1 clears the event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							
F	RW W1C	EVENTCHGERROR			Event charging error. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							

7.7.1.12 INTENEVENTSBCHARGER1SET

Address offset: 0xC

Battery Charger Status Events Interrupt Enable Set

Bit number					7	6	5	4	3	2	1	0
ID						F	E	D	C	B	A	
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1S	EVENTSUPPLEMENT			Writing 1 enables interrupts from EVENTSUPPLEMENT							
			LOW	0	low							
			HIGH	1	high							
B	RW W1S	EVENTCHGTRICKLE			Writing 1 enables interrupts from EVENTCHGTRICKLE							
			LOW	0	low							
			HIGH	1	high							
C	RW W1S	EVENTCHGCC			Writing 1 enables interrupts from EVENTCHGCC							
			LOW	0	low							
			HIGH	1	high							
D	RW W1S	EVENTCHGCV			Writing 1 enables interrupts from EVENTCHGCV							
			LOW	0	low							

Bit number					7	6	5	4	3	2	1	0
ID							F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
			HIGH	1	high							
E	RW W1S	EVENTCHGCOMPLETED			Writing 1 enables interrupts from EVENTCHGCOMPLETED							
			LOW	0	low							
			HIGH	1	high							
F	RW W1S	EVENTCHGERROR			Writing 1 enables interrupts from EVENTCHGERROR							
			LOW	0	low							
			HIGH	1	high							

7.7.1.13 INTENEVENTSBCHARGER1CLR

Address offset: 0xD

Battery Charger Status Events Interrupt Enable Clear

Bit number					7	6	5	4	3	2	1	0
ID							F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1C	EVENTSUPPLEMENT			Writing 1 disables interrupts from EVENTSUPPLEMENT							
			LOW	0	low							
			HIGH	1	high							
B	RW W1C	EVENTCHGTRICKLE			Writing 1 disables interrupts from EVENTCHGTRICKLE							
			LOW	0	low							
			HIGH	1	high							
C	RW W1C	EVENTCHGCC			Writing 1 disables interrupts from EVENTCHGCC							
			LOW	0	low							
			HIGH	1	high							
D	RW W1C	EVENTCHGCV			Writing 1 disables interrupts from EVENTCHGCV							
			LOW	0	low							
			HIGH	1	high							
E	RW W1C	EVENTCHGCOMPLETED			Writing 1 disables interrupts from EVENTCHGCOMPLETED							
			LOW	0	low							
			HIGH	1	high							
F	RW W1C	EVENTCHGERROR			Writing 1 disables interrupts from EVENTCHGERROR							
			LOW	0	low							
			HIGH	1	high							

7.7.1.14 EVENTSBCHARGER2SET

Address offset: 0xE

Battery Charger Battery Events Event Set

Bit number					7	6	5	4	3	2	1	0
ID										C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1S	EVENTBATDETECTED			Event Battery Detected. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							
B	RW W1S	EVENTBATLOST			Event Battery Lost. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							
C	RW W1S	EVENTBATRECHARGE			Event Battery re-charge needed. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							

7.7.1.15 EVENTSBCHARGER2CLR

Address offset: 0xF

Battery Charger Battery Events Event Clear

Bit number					7	6	5	4	3	2	1	0
ID										C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1C	EVENTBATDETECTED			Event Battery Detected. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							
B	RW W1C	EVENTBATLOST			Event Battery Lost. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							
C	RW W1C	EVENTBATRECHARGE			Event Battery re-charge needed. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							

7.7.1.16 INTENEVENTSBCHARGER2SET

Address offset: 0x10

Battery Charger Battery Events Interrupt Enable Set

Bit number					7	6	5	4	3	2	1	0
ID										C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1S	EVENTBATDETECTED			Writing 1 enables interrupts from EVENTBATDETECTED							
			LOW	0	low							
			HIGH	1	high							
B	RW W1S	EVENTBATLOST			Writing 1 enables interrupts from EVENTBATLOST							
			LOW	0	low							
			HIGH	1	high							
C	RW W1S	EVENTBATRECHARGE			Writing 1 enables interrupts from EVENTBATRECHARGE							
			LOW	0	low							
			HIGH	1	high							

7.7.1.17 INTENEVENTSBCHARGER2CLR

Address offset: 0x11

Battery Charger Battery Events Interrupt Enable Clear

Bit number					7	6	5	4	3	2	1	0
ID										C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1C	EVENTBATDETECTED			Writing 1 disables interrupts from EVENTBATDETECTED							
			LOW	0	low							
			HIGH	1	high							
B	RW W1C	EVENTBATLOST			Writing 1 disables interrupts from EVENTBATLOST							
			LOW	0	low							
			HIGH	1	high							
C	RW W1C	EVENTBATRECHARGE			Writing 1 disables interrupts from EVENTBATRECHARGE							
			LOW	0	low							
			HIGH	1	high							

7.7.1.18 EVENTSSHPHLDSET

Address offset: 0x12

ShipHold pin Events Event Set

Bit number					7	6	5	4	3	2	1	0
ID									D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1S	EVENTSHPHLDBTNPRESS			Event when Ship-Hold button is pressed. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							

Bit number					7	6	5	4	3	2	1	0
ID									D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
B	RW W1S	EVENTSHPHLDBTNRE			Event when Ship-Hold button is Released. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							
C	RW W1S	EVENTSHPHLDEXIT			Event when Ship-Hold button held to Exit. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							
D	RW W1S	EVENTWATCHDOGW			Event when Watchdog Timeout Warning detected. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							

7.7.1.19 EVENTSSHPHLDCLR

Address offset: 0x13

ShipHold pin Events Event Clear

Bit number					7	6	5	4	3	2	1	0
ID									D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1C	EVENTSHPHLDBTNPRESS			Event when Ship-Hold button is pressed. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							
B	RW W1C	EVENTSHPHLDBTNRE			Event when Ship-Hold button is Released. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							
C	RW W1C	EVENTSHPHLDEXIT			Event when Ship-Hold button held to Exit. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							
D	RW W1C	EVENTWATCHDOGW			Event when Watchdog Timeout Warning detected. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							

7.7.1.20 INTENEVENTSSHPHLDSET

Address offset: 0x14

ShipHold pin Events Interrupt Enable Set

Bit number					7	6	5	4	3	2	1	0
ID									D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1S	EVENTSHPHLDBTNPRESS			Writing 1 enables interrupts from EVENTSHPHLDBTNPRESS							
			LOW	0	low							
			HIGH	1	high							
B	RW W1S	EVENTSHPHLDBTNRE			Writing 1 enables interrupts from EVENTSHPHLDBTNRELEASE							
			LOW	0	low							
			HIGH	1	high							
C	RW W1S	EVENTSHPHLDEXIT			Writing 1 enables interrupts from EVENTSHPHLDEXIT							
			LOW	0	low							
			HIGH	1	high							
D	RW W1S	EVENTWATCHDOGW			Writing 1 enables interrupts from EVENTWATCHDOGWARN							
			LOW	0	low							
			HIGH	1	high							

7.7.1.21 INTENEVENTSSHPHLDCLR

Address offset: 0x15

ShipHold pin Events Interrupt Enable Clear

Bit number					7	6	5	4	3	2	1	0
ID									D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1C	EVENTSHPHLDBTNPRESS			Writing 1 disables interrupts from EVENTSHPHLDBTNPRESS							
			LOW	0	low							
			HIGH	1	high							
B	RW W1C	EVENTSHPHLDBTNRE			Writing 1 disables interrupts from EVENTSHPHLDBTNRELEASE							
			LOW	0	low							
			HIGH	1	high							
C	RW W1C	EVENTSHPHLDEXIT			Writing 1 disables interrupts from EVENTSHPHLDEXIT							
			LOW	0	low							
			HIGH	1	high							
D	RW W1C	EVENTWATCHDOGW			Writing 1 disables interrupts from EVENTWATCHDOGWARN							
			LOW	0	low							
			HIGH	1	high							

7.7.1.22 EVENTSVBUSIN0SET

Address offset: 0x16

VBUSIN Voltage Detection Events Event Set

Bit number					7	6	5	4	3	2	1	0
ID							F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1S	EVENTVBUSDETECTED			Event VBUS input detected. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							
B	RW W1S	EVENTVBUSREMOVE			Event VBUS input removed. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							
C	RW W1S	EVENTVBUSOVRVOLTDETECTED			Event VBUS Over Voltage Detected. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							
D	RW W1S	EVENTVBUSOVRVOL			Event VBUS Over Removed. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							
E	RW W1S	EVENTVBUSUNDVOLTDETECTED			Event VBUS Under Voltage Detected. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							
F	RW W1S	EVENTVBUSUNDVOL			Event VBUS Under Removed. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							

7.7.1.23 EVENTSVBUSIN0CLR

Address offset: 0x17

VBUSIN Voltage Detection Events Event Clear

Bit number					7	6	5	4	3	2	1	0
ID							F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1C	EVENTVBUSDETECTED			Event VBUS input detected. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							
B	RW W1C	EVENTVBUSREMOVE			Event VBUS input removed. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							
C	RW W1C	EVENTVBUSOVRVOLTDETECTED			Event VBUS Over Voltage Detected. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							
D	RW W1C	EVENTVBUSOVRVOL			Event VBUS Over Removed. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
			LOW	0	low							

Bit number					7	6	5	4	3	2	1	0
ID							F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
			HIGH	1	high							
E	RW W1C	EVENTVBUSUNDVOLTDETECTED			Event VBUS Under Voltage Detected. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							
F	RW W1C	EVENTVBUSUNDVOL			Event VBUS Under Removed. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							

7.7.1.24 INTENEVENTSVBUSIN0SET

Address offset: 0x18

VBUSIN Voltage Detection Events Interrupt Enable Set

Bit number					7	6	5	4	3	2	1	0
ID							F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1S	EVENTVBUSDETECTED			Writing 1 enables interrupts from EVENTVBUSDETECTED							
			LOW	0	low							
			HIGH	1	high							
B	RW W1S	EVENTVBUSREMOVE			Writing 1 enables interrupts from EVENTVBUSREMOVED							
			LOW	0	low							
			HIGH	1	high							
C	RW W1S	EVENTVBUSOVRVOLTDETECTED			Writing 1 enables interrupts from EVENTVBUSOVRVOLTDETECTED							
			LOW	0	low							
			HIGH	1	high							
D	RW W1S	EVENTVBUSOVRVOL			Writing 1 enables interrupts from EVENTVBUSOVRVOLTREMOVED							
			LOW	0	low							
			HIGH	1	high							
E	RW W1S	EVENTVBUSUNDVOLTDETECTED			Writing 1 enables interrupts from EVENTVBUSUNDVOLTDETECTED							
			LOW	0	low							
			HIGH	1	high							
F	RW W1S	EVENTVBUSUNDVOL			Writing 1 enables interrupts from EVENTVBUSUNDVOLTREMOVED							
			LOW	0	low							
			HIGH	1	high							

7.7.1.25 INTENEVENTSVBUSIN0CLR

Address offset: 0x19

VBUSIN Voltage Detection Events Interrupt Enable Clear

Bit number					7	6	5	4	3	2	1	0
ID							F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1C	EVENTVBUSDETECTED			Writing 1 disables interrupts from EVENTVBUSDETECTED							
			LOW	0	low							
			HIGH	1	high							
B	RW W1C	EVENTVBUSREMOVE			Writing 1 disables interrupts from EVENTVBUSREMOVED							
			LOW	0	low							
			HIGH	1	high							
C	RW W1C	EVENTVBUSOVRVOLTDETECTED			Writing 1 disables interrupts from EVENTVBUSOVRVOLTDETECTED							
			LOW	0	low							
			HIGH	1	high							
D	RW W1C	EVENTVBUSOVRVOL			Writing 1 disables interrupts from EVENTVBUSOVRVOLTREMOVED							
			LOW	0	low							
			HIGH	1	high							
E	RW W1C	EVENTVBUSUNDVOLTDETECTED			Writing 1 disables interrupts from EVENTVBUSUNDVOLTDETECTED							
			LOW	0	low							
			HIGH	1	high							
F	RW W1C	EVENTVBUSUNDVOL			Writing 1 disables interrupts from EVENTVBUSUNDVOLTREMOVED							
			LOW	0	low							
			HIGH	1	high							

7.7.1.26 EVENTSVBUSIN1SET

Address offset: 0x1A

VBUSIN Thermal and USB Events Event Set

Bit number					7	6	5	4	3	2	1	0
ID							F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1S	EVENTTHERMALWARNDETECTED			Event Thermal Warning detected. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							
B	RW W1S	EVENTTHERMALWAF			Event Thermal Warning removed. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							
C	RW W1S	EVENTTHERMALSHUTDOWNDETECTED			Event Thermal Shutown detected. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							
D	RW W1S	EVENTTHERMALSHU			Event Thermal Shutdown removed. Writing 1 sets the event (for debugging).							
			LOW	0	low							

Bit number					7	6	5	4	3	2	1	0
ID							F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
			HIGH	1	high							
E	RW W1S	EVENTCC1STATECHANGE			Event when Voltage on CC1 changes. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							
F	RW W1S	EVENTCC2STATECHA			Event when Voltage on CC2 changes. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							

7.7.1.27 EVENTSVBUSIN1CLR

Address offset: 0x1B

VBUSIN Thermal and USB Events Event Clear

Bit number					7	6	5	4	3	2	1	0
ID							F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1C	EVENTTHERMALWARNDETECTED			Event Thermal Warning detected. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							
B	RW W1C	EVENTTHERMALWAF			Event Thermal Warning removed. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							
C	RW W1C	EVENTTHERMALSHUTDOWNDETECTED			Event Thermal Shutown detected. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							
D	RW W1C	EVENTTHERMALSHU			Event Thermal Shutdown removed. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							
E	RW W1C	EVENTCC1STATECHANGE			Event when Voltage on CC1 changes. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							
F	RW W1C	EVENTCC2STATECHA			Event when Voltage on CC2 changes. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							

7.7.1.28 INTENEVENTSVBUSIN1SET

Address offset: 0x1C

VBUSIN Thermal and USB Events Interrupt Enable Set

Bit number					7	6	5	4	3	2	1	0
ID							F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1S	EVENTTHERMALWARNDETECTED			Writing 1 enables interrupts from EVENTTHERMALWARNDETECTED							
			LOW	0	low							
			HIGH	1	high							
B	RW W1S	EVENTTHERMALWAF			Writing 1 enables interrupts from EVENTTHERMALWARNREMOVED							
			LOW	0	low							
			HIGH	1	high							
C	RW W1S	EVENTTHERMALSHUTDOWNDETECTED			Writing 1 enables interrupts from EVENTTHERMALSHUTDOWNDETECTED							
			LOW	0	low							
			HIGH	1	high							
D	RW W1S	EVENTTHERMALSHU			Writing 1 enables interrupts from EVENTTHERMALSHUTDOWNREMOVED							
			LOW	0	low							
			HIGH	1	high							
E	RW W1S	EVENTCC1STATECHANGE			Writing 1 enables interrupts from EVENTCC1STATECHANGE							
			LOW	0	low							
			HIGH	1	high							
F	RW W1S	EVENTCC2STATECHA			Writing 1 enables interrupts from EVENTCC2STATECHANGE							
			LOW	0	low							
			HIGH	1	high							

7.7.1.29 INTENEVENTSVBUSIN1CLR

Address offset: 0x1D

VBUSIN Thermal and USB Events Interrupt Enable Clear

Bit number					7	6	5	4	3	2	1	0
ID							F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1C	EVENTTHERMALWARNDETECTED			Writing 1 disables interrupts from EVENTTHERMALWARNDETECTED							
			LOW	0	low							
			HIGH	1	high							
B	RW W1C	EVENTTHERMALWAF			Writing 1 disables interrupts from EVENTTHERMALWARNREMOVED							
			LOW	0	low							
			HIGH	1	high							
C	RW W1C	EVENTTHERMALSHUTDOWNDETECTED			Writing 1 disables interrupts from EVENTTHERMALSHUTDOWNDETECTED							
			LOW	0	low							
			HIGH	1	high							
D	RW W1C	EVENTTHERMALSHU			Writing 1 disables interrupts from EVENTTHERMALSHUTDOWNREMOVED							
			LOW	0	low							

Bit number					7	6	5	4	3	2	1	0
ID							F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
			HIGH	1	high							
E	RW W1C	EVENTCC1STATECHANGE			Writing 1 disables interrupts from EVENTCC1STATECHANGE							
			LOW	0	low							
			HIGH	1	high							
F	RW W1C	EVENTCC2STATECHA			Writing 1 disables interrupts from EVENTCC2STATECHANGE							
			LOW	0	low							
			HIGH	1	high							

7.7.1.30 EVENTSGPIOSET

Address offset: 0x22

GPIO Event Event Set

Bit number					7	6	5	4	3	2	1	0
ID								E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1S	EVENTGPIOEDGEDETECT0			Event when GPIO input 0 edge is detected. GPIOS.GPIO_MODE = 3 : Rising Edge GPIOS.GPIO_MODE = 4 : Falling Edge. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							
B	RW W1S	EVENTGPIOEDGEDET			Event when GPIO input 1 edge is detected. GPIOS.GPIO_MODE = 3 : Rising Edge GPIOS.GPIO_MODE = 4 : Falling Edge. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							
C	RW W1S	EVENTGPIOEDGEDETECT2			Event when GPIO input 2 edge is detected. GPIOS.GPIO_MODE = 3 : Rising Edge GPIOS.GPIO_MODE = 4 : Falling Edge. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							
D	RW W1S	EVENTGPIOEDGEDET			Event when GPIO input 3 edge is detected. GPIOS.GPIO_MODE = 3 : Rising Edge GPIOS.GPIO_MODE = 4 : Falling Edge. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							
E	RW W1S	EVENTGPIOEDGEDETECT4			Event when GPIO input 4 edge is detected. GPIOS.GPIO_MODE = 3 : Rising Edge GPIOS.GPIO_MODE = 4 : Falling Edge. Writing 1 sets the event (for debugging).							
			LOW	0	low							
			HIGH	1	high							

7.7.1.31 EVENTSGPIOCLR

Address offset: 0x23

GPIO Event Event Clear

Bit number					7	6	5	4	3	2	1	0
ID								E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1C	EVENTGPIOEDGEDETECT0			Event when GPIO input 0 edge is detected. GPIOS.GPIO_MODE = 3 : Rising Edge GPIOS.GPIO_MODE = 4 : Falling Edge. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							
B	RW W1C	EVENTGPIOEDGEDET			Event when GPIO input 1 edge is detected. GPIOS.GPIO_MODE = 3 : Rising Edge GPIOS.GPIO_MODE = 4 : Falling Edge. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							
C	RW W1C	EVENTGPIOEDGEDETECT2			Event when GPIO input 2 edge is detected. GPIOS.GPIO_MODE = 3 : Rising Edge GPIOS.GPIO_MODE = 4 : Falling Edge. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							
D	RW W1C	EVENTGPIOEDGEDET			Event when GPIO input 3 edge is detected. GPIOS.GPIO_MODE = 3 : Rising Edge GPIOS.GPIO_MODE = 4 : Falling Edge. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							
E	RW W1C	EVENTGPIOEDGEDETECT4			Event when GPIO input 4 edge is detected. GPIOS.GPIO_MODE = 3 : Rising Edge GPIOS.GPIO_MODE = 4 : Falling Edge. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
			LOW	0	low							
			HIGH	1	high							

7.7.1.32 INTENEVENTSGPIOSET

Address offset: 0x24

GPIO Event Interrupt Enable Set

Bit number					7	6	5	4	3	2	1	0
ID								E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1S	EVENTGPIOEDGEDETECT0			Writing 1 enables interrupts from EVENTGPIOEDGEDETECT0							
			LOW	0	low							
			HIGH	1	high							
B	RW W1S	EVENTGPIOEDGEDET			Writing 1 enables interrupts from EVENTGPIOEDGEDETECT1							
			LOW	0	low							
			HIGH	1	high							
C	RW W1S	EVENTGPIOEDGEDETECT2			Writing 1 enables interrupts from EVENTGPIOEDGEDETECT2							
			LOW	0	low							
			HIGH	1	high							
D	RW W1S	EVENTGPIOEDGEDET			Writing 1 enables interrupts from EVENTGPIOEDGEDETECT3							

Bit number						7	6	5	4	3	2	1	0
ID									E	D	C	B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
			LOW	0	low								
			HIGH	1	high								
E	RW W1S	EVENTGPIOEDGEDETECT4			Writing 1 enables interrupts from EVENTGPIOEDGEDETECT4								
			LOW	0	low								
			HIGH	1	high								

7.7.1.33 INTENEVENTSGPIOCLR

Address offset: 0x25

GPIO Event Interrupt Enable Clear

Bit number						7	6	5	4	3	2	1	0
ID									E	D	C	B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW W1C	EVENTGPIOEDGEDETECT0			Writing 1 disables interrupts from EVENTGPIOEDGEDETECT0								
			LOW	0	low								
			HIGH	1	high								
B	RW W1C	EVENTGPIOEDGEDET			Writing 1 disables interrupts from EVENTGPIOEDGEDETECT1								
			LOW	0	low								
			HIGH	1	high								
C	RW W1C	EVENTGPIOEDGEDETECT2			Writing 1 disables interrupts from EVENTGPIOEDGEDETECT2								
			LOW	0	low								
			HIGH	1	high								
D	RW W1C	EVENTGPIOEDGEDET			Writing 1 disables interrupts from EVENTGPIOEDGEDETECT3								
			LOW	0	low								
			HIGH	1	high								
E	RW W1C	EVENTGPIOEDGEDETECT4			Writing 1 disables interrupts from EVENTGPIOEDGEDETECT4								
			LOW	0	low								
			HIGH	1	high								

7.8 Reset and error registers

This section details the error and reset related registers.

Note: During the cooling period after a TSD and if VSYS drops below VSYSCOMP, VSYSLOW could be set instead of THERMALSHUTDOWN in register RSTCAUSE on page 123.

7.8.1 Registers

Instances

Instance	Base address	Description
ERRLOG	0x00000E00	Error Log Registers ERRLOG register map

Register overview

Register	Offset	Description
TASKCLRERRLOG	0x0	task to clear the Errlog registers
SCRATCH0	0x1	Scratch register 0
SCRATCH1	0x2	Scratch register 1
RSTCAUSE	0x3	Error log for internal reset causes. Cleared withTASK_CLR_ERRLOG
CHARGERERRREASON	0x4	Error log for slowDomain. Cleared with TASK_CLR_ERRLOG
CHARGERERRSENSOR	0x5	Bcharger Fsm sensor error. Cleared with TASK_CLR_ERRLOG

7.8.1.1 TASKCLRERRLOG

Address offset: 0x0

task to clear the Errlog registers

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TASKCLRERRLOG			Clear Errlog								

7.8.1.2 SCRATCH0

Address offset: 0x1

Scratch register 0

Bit number						7	6	5	4	3	2	1	0
ID						B	B	B	B	B	B	B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	BOOTTIMEREN			Enable Boot Monitor Timer, only cleared by POR								
			NOBOOTMON	0	bootMonitor disable								
			BOOTMON	1	bootMonitor enable								
B	RW	SCRATCH0			scratch register, only cleared by POR								

7.8.1.3 SCRATCH1

Address offset: 0x2

Scratch register 1

Bit number					7	6	5	4	3	2	1	0
ID					A	A	A	A	A	A	A	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	SCRATCH1			scratch register, only cleared by POR							

7.8.1.4 RSTCAUSE

Address offset: 0x3

Error log for internal reset causes. Cleared withTASK_CLR_ERRLOG

Bit number					7	6	5	4	3	2	1	0
ID						G	F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	R	SHIPMODEEXIT			internal reset caused by shipmode exit							
			NORST	0	no shipmode reset							
			RST	1	reset activated by shipmode exit							
B	R	BOOTMONITORTIME			internal reset caused by boot monitor timeout							
			NORST	0	no bootMonitor reset							
			RST	1	reset activated by bootMonitor							
C	R	WATCHDOGTIMEOUT			internal reset caused by watchdog timeout							
			NORST	0	no watchdog reset							
			RST	1	reset activated by watchdog							
D	R	LONGPRESSTIMEOUT			internal reset caused by shphld long press							
			NORST	0	no long press reset							
			RST	1	Reset activated by long press of SHPHLD or SHPHLD+GPIO							
E	R	THERMALSHUTDOWN			internal reset caused by TSD							
			NORST	0	no TSD reset							
			RST	1	reset activated by TSD							
F	R	VSYSLOW			internal reset caused by POF, VSYS low							
			NORST	0	no VSYS low reset							
			RST	1	reset activated by VSYS low							
G	R	SWRESET			internal reset caused by soft reset							
			NORST	0	no s/w reset							
			RST	1	reset activated by s/w reset							

7.8.1.5 CHARGERERRREASON

Address offset: 0x4

Error log for slowDomain. Cleared with TASK_CLR_ERRLOG

Bit number					7	6	5	4	3	2	1	0
ID						G	F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	R	NTCSENSORERR			NTC thermistor sensor error							
B	R	VBATSENSORERR			VBAT Sensor Error							
C	R	VBATLOW			VBAT Low Error							
D	R	VTRICKLE			Vtrickle Error							
E	R	MEASTIMEOUT			Measurement Timeout Error							
F	R	CHARGETIMEOUT			Charge Timeout Error							
G	R	TRICKLETIMEOUT			Trickle Timeout Error							

7.8.1.6 CHARGERERRSENSOR

Address offset: 0x5

Bcharger Fsm sensor error. Cleared with TASK_CLR_ERRLOG

Bit number						7	6	5	4	3	2	1	0
ID						H	G	F	E	D	C	B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	R	SENSORNTCCOLD			NTC thermistor Cold sensor value during error								
B	R	SENSORNTCCOOL			NTC thermistor Cool sensor value during error								
C	R	SENSORNTCWARM			NTC thermistor Warm sensor value during error								
D	R	SENSORNTCHOT			NTC thermistor Hot sensor value during error								
E	R	SENSORVTERM			Vterm sensor value during error								
F	R	SENSORRECHARGE			Recharge sensor value during error								
G	R	SENSORVTRICKLE			Vtrickle sensor value during error								
H	R	SENSORVBATLOW			VbatLow sensor value during error								

8 Application

The following application example uses nPM1300 and an nRF5x wireless System on Chip (SoC). An nRF52 or nRF53 series device with USB can be configured in the same way. For other configurations, see Reference circuitry on page 132.

The example application is for a design with the following configuration and features:

- BUCK[n], LOADSW, and LDO are in use
- Host software controls the device through TWI, the interrupt pin **INT**, and the interrupt on the **GPIO0** pin
- Three LEDs available
- NTC thermistor in the battery pack
- Ship mode
- Battery monitoring circuit and low battery indication LED

8.1 Schematic

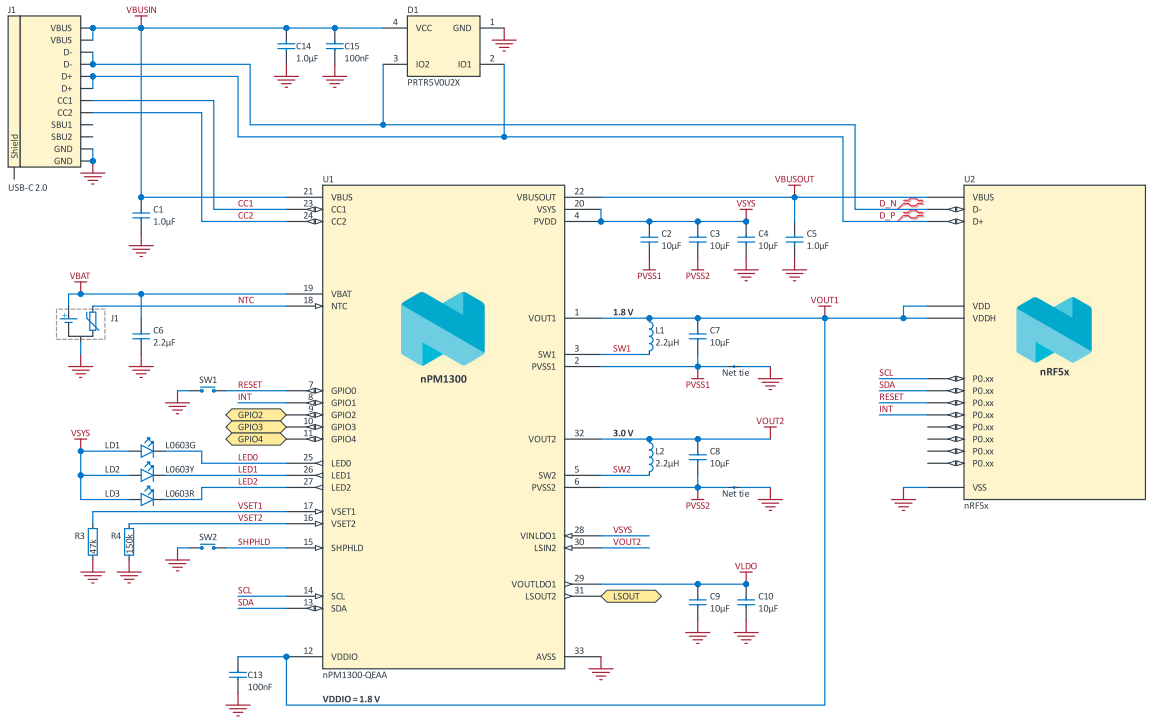

Figure 19: Application example

8.2 Supplying from BUCK

An application must not be supplied directly from **VBAT**. This can interrupt the battery charging process causing incorrect behavior from the charger. Use either **VOUT1**, **VOUT2**, or **VSYS** to supply the application.

BUCK1 starts automatically and supplies the nRF5x host SoC with 1.8 V. BUCK1 is the I/O voltage for the system. BUCK2 starts automatically (3 V) and is available for customizable features.

8.3 USB port negotiation

nRF5x can connect to a USB host.

Port negotiation is performed after nPM1300 port detection. The nRF5x device and nPM1300 are both connected to USB-C in the application example.

- The **D+** and **D–** pins are connected to nRF5x. The **CC1** and **CC2** pins are connected to nPM1300. The nRF5x SoC must wait until nPM1300 completes port detection using the USB configuration channel.
- The nRF5x must set the correct current limit as described in Charge current limit (ICHG) on page 25.
- **VBUS** is supplied to SYSREG on nPM1300 and **VBUSOUT** supplies the nRF5x **VBUS** source.

8.4 Charging and error states

Three LEDs can be used for charging indicators or general purpose by the application.

8.5 Termination voltage and current

The termination voltage, V_{TERM}, is configured through TWI up to 4.45 V.

Charge current is configured through TWI.

8.6 NTC thermistor configuration

The **NTC** pin is connected to an external NTC thermistor. Place the NTC thermistor with thermal coupling on the battery pack.

8.7 Ship mode

Ship mode is enabled at production time through the TWI interface.

SHPHLD is connected to **SW2**. The external button is in the circuit to exit Ship mode. If another circuit is present instead of a button, any signal that is able to pull the **SHPHLD** pin low for the required period can be connected to that net. See Ship and Hibernate modes on page 94 for more information.

9 Hardware and layout

9.1 Pin assignments

The pin assignment figures and tables describe the pinouts for the product variants of the chip.

9.1.1 QFN32 pin assignments

The pin assignment figure and table describe the assignments for this variant of the chip.

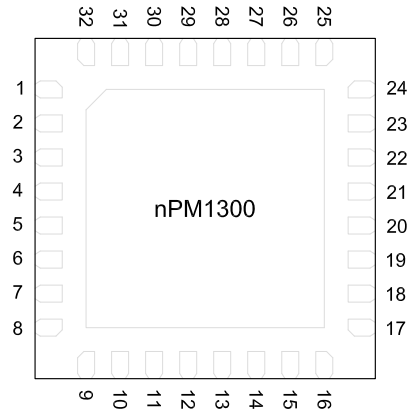

Figure 20: QFN32 pin assignments (top view)

Pin	Name	Function	Description
1	VOUT1	Power	BUCK1 output
2	PVSS1	Power	BUCK1 power ground
3	SW1	Power	BUCK1 regulator output (to inductor)
4	PVDD	Power	BUCK[1..2] power input
5	SW2	Power	BUCK2 regulator output (to inductor)
6	PVSS2	Power	BUCK2 power ground
7	GPIO0	Digital I/O	GPIO0
8	GPIO1	Digital I/O	GPIO1
9	GPIO2	Digital I/O	GPIO2
10	GPIO3	Digital I/O	GPIO3
11	GPIO4	Digital I/O	GPIO4
12	VDDIO	Power	Supply for TWI and GPIOs
13	SDA	Digital I/O	TWI data
14	SCL	Digital input	TWI clock
15	SHPHLD	Digital input	Ship mode hold
16	VSET2	Analog input	Voltage set for BUCK2 (to resistor)
17	VSET1	Analog input	Voltage set for BUCK1 (to resistor)
18	NTC	Analog input	Battery thermistor
19	VBAT	Power	Battery
20	VSYS	Power	System voltage output
21	VBUS	Power	Input supply
22	VBUSOUT	Analog output	VBUS output for host
23	CC1	Analog input	USB Type-C configuration channel 1
24	CC2	Analog input	USB Type-C configuration channel 2
25	LED0	Analog output	LEDDRV0 output
26	LED1	Analog output	LEDDRV1 output
27	LED2	Analog output	LEDDRV2 output
28	LSIN1/ VINLDO1	Power	LOADSW1 supply or LDO1 input
29	LSOUT1/ VOUTLDO1	Power	LOADSW1 or LDO1 output
30	LSIN2/ VINLDO2	Power	LOADSW2 supply or LDO2 input
31	LSOUT2/ VOUTLDO2	Power	LOADSW2 or LDO2 output
32	VOUT2	Power	BUCK2 output

Pin	Name	Function	Description
Exposed pad	AVSS	Power	Ground

Table 32: QFN32 pin assignments

9.1.2 WLCSP ball assignments

The ball assignment figure and table describe the ball assignments for this variant of the chip.

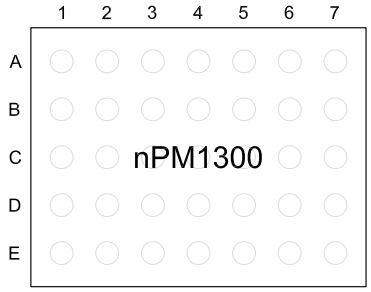

Figure 21: WLCSP ball assignment (top view)

Ball	Name	Function	Description
A1	LED0	Analog output	LEDDRV0 output
A2	LED1	Analog output	LEDDRV1 output
A3	LED2	Analog output	LEDDRV2 output
A4	LSOUT1/ VOUTLDO1	Power	LOADSW1 or LDO1 output
A5	LSOUT2/ VOUTLDO2	Power	LOADSW2 or LDO2 output
A6	AVSS	Power	Ground
A7	PVSS1	Power	BUCK1 power ground
B1, B2	VBUS	Power	Input supply
B3	CC2	Analog input	USB Type-C configuration channel 2
B4	LSIN1/ VINLDO1	Power	LOADSW1 supply or LDO1 input
B5	LSIN2/ VINLDO2	Power	LOADSW2 supply or LDO2 input
B6	VOUT1	Power	BUCK1 output
B7	SW1	Power	BUCK1 regulator output (to inductor)
C1, C2	VSYS	Power	System voltage output
C3	VBUSOUT	Analog output	VBUS output for host
C4	GPIO3	Digital I/O	GPIO3
C5	GPIO2	Digital I/O	GPIO2
C6	VOUT2	Power	BUCK2 output
C7	PVDD	Power	Power input for BUCK[1..2]
D1, D2	VBAT	Power	Battery
D3	NTC	Analog input	Battery thermistor
D4	SHPHLD	Digital input	Ship mode hold
D5	CC1	Analog input	USB Type-C configuration channel 1
D6	GPIO0	Digital I/O	GPIO0
D7	SW2	Power	BUCK2 regulator output (to inductor)
E1	VSET2	Analog input	Voltage set for BUCK2 (to resistor)
E2	VSET1	Analog input	Voltage set for BUCK1 (to resistor)
E3	SCL	Digital input	TWI clock
E4	VDDIO	Power	Supply for TWI and GPIOs
E5	SDA	Digital I/O	TWI data
E6	GPIO1	Digital I/O	GPIO1

Ball	Name	Function	Description
E7	PVSS2	Power	BUCK2 power ground

Table 33: Pin descriptions

9.2 Mechanical specifications

The mechanical specifications for the packages show the dimensions in millimeters.

9.2.1 QFN32 5x5 mm package

Dimensions in millimeters for the QFN32 5.0x5.0 mm package.

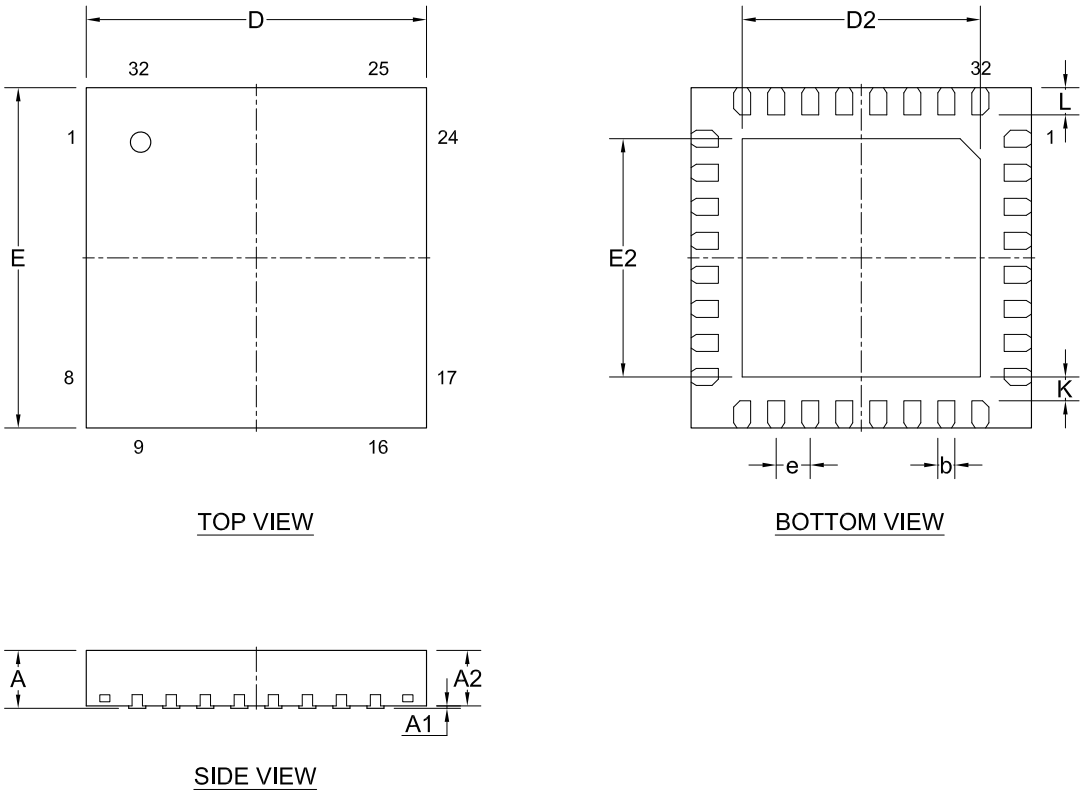

Figure 22: QFN32 5.0x5.0 mm package

	A	A1	A2	A3	b	D	D2	E	E2	e	K	L
Min.	0.8	0			0.2		3.4		3.4			0.3
Nom.	0.85	0.035	0.815		0.25	5	3.5	5	3.5	0.5	0.7	0.4
Max.	0.9	0.05			0.3		3.6		3.6			0.45

Table 34: QFN32 dimensions in millimeters

9.2.2 WLCSP package

Dimensions in millimeters for the WLCSP 2.3775x3.0775 mm package.

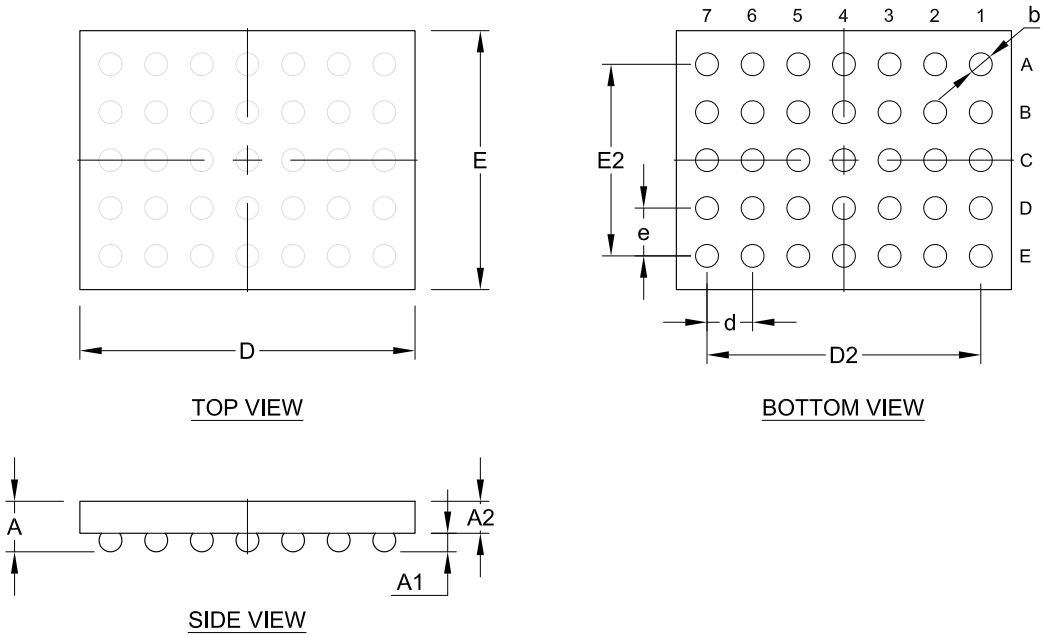

Figure 23: WLCSP 2.3775x3.0775 mm package

	A	A1	A2	A3	D	D2	d	E	E2	e	b	n
Min.	0.416	0.14	0.254	0.022							0.195	
Nom.	0.464		0.269	0.025	3.0775	2.514	0.419	2.3775	1.76	0.44		35
Max.	0.512	0.2	0.284	0.028							0.255	

Table 35: WLCSP dimensions in millimeters

9.3 Reference circuitry

Documentation for the different package reference circuits, including Altium Designer files, PCB layout files, and PCB production files, can be downloaded from www.nordicsemi.com.

The following reference circuits for the nPM1300 QFN package show the schematics and components to support different configurations in a design.

	Configuration 1	Configuration 2	Configuration 3
Description	Full configuration	Simple configuration	Minimal configuration
BUCKs	Both configured	One configured	Not used
LOADSWs	Both configured, LDO mode	One configured, load switch mode	Not used
Ship mode exit	Configured	Configured	Not used
Charging	Available	Available	Available
Battery thermistor	Configured	Configured	Not used
LEDs	Three available	One available	Not used
GPIOs	Configured	Configured	Configured
TWI	Configured	Configured	Configured
VSET1	47 kΩ ±1%	47 kΩ ±1%	Not used
VSET2	150 kΩ ±1%		Not used
VOUT1	1.8 V	1.8 V	Not used
VOUT2	3.0 V	Not used	Not used
VBUSOUT	Configured	Configured	Not used
VDDIO	Configured	Configured	Configured

Table 36: PCB application configuration

9.3.1 Configuration 1

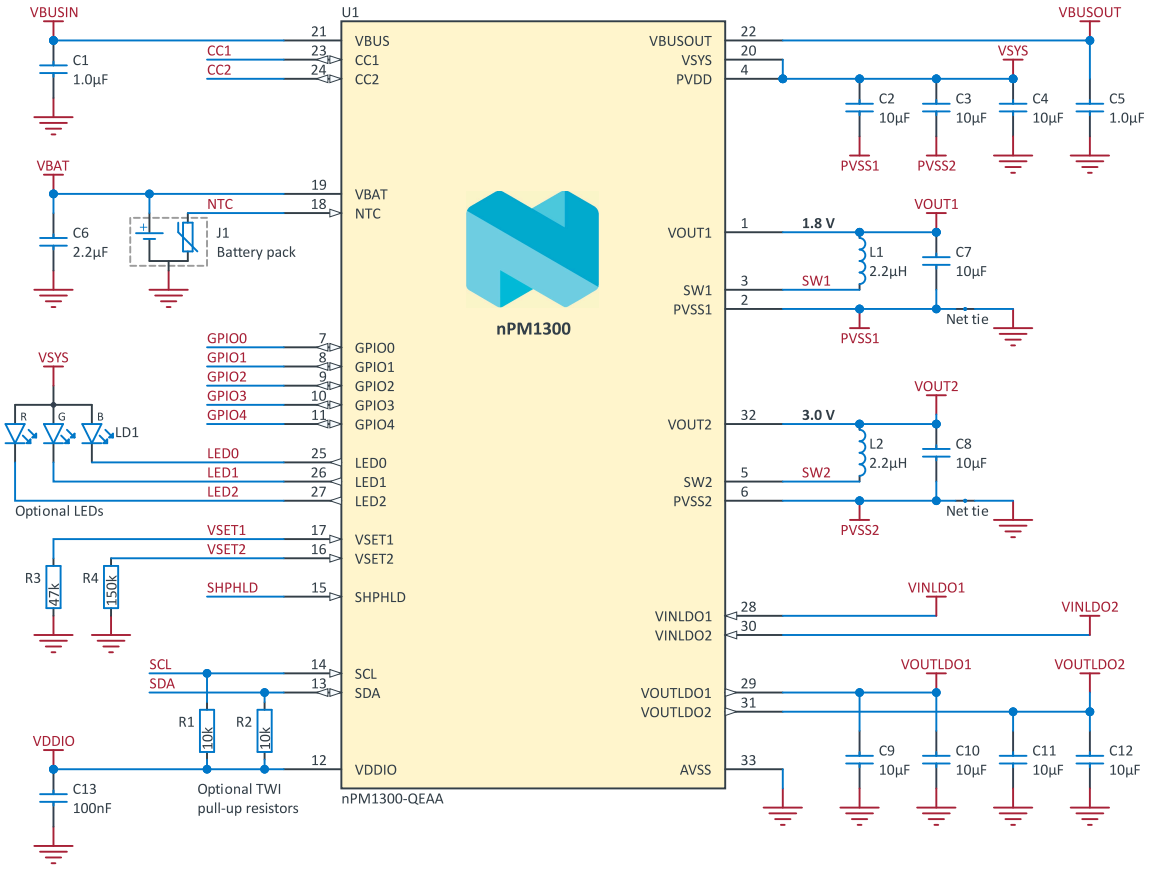

Figure 24: QFN schematic

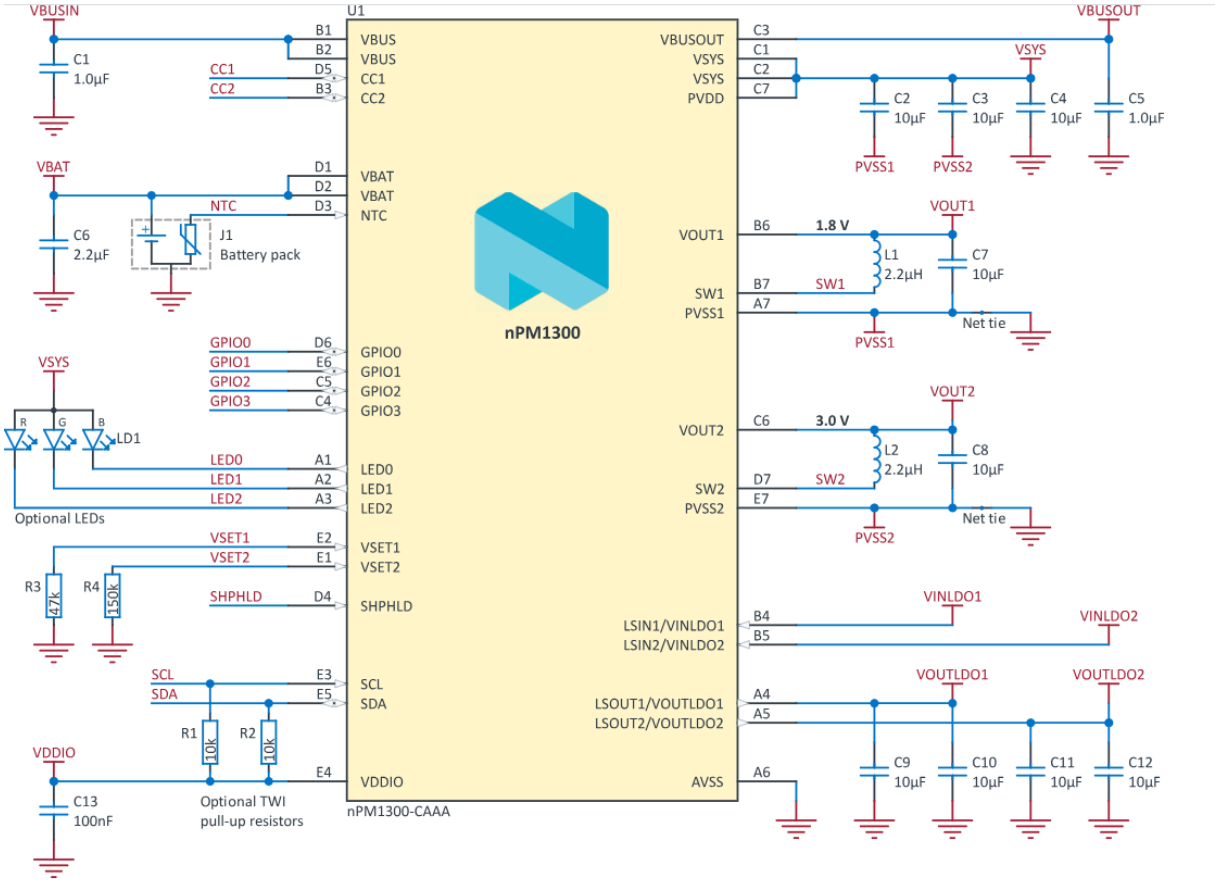

Figure 25: WLCSP schematic

Designator	Value	Description	Footprint
C1, C5	1.0 µF	Capacitor, X5R, 10 V, ±10%	0603
C2, C3, C4, C7, C8, C9, C10, C11, C12	10 µF	Capacitor, X5R, 25 V, ±20%	0603
C6	2.2 µF	Capacitor, X7R, 16 V, ±10%	0603
C13	100 nF	Capacitor, X5R, ±10%	0201
L1, L2	2.2 µH	Inductor, DCR < 400 mΩ, ±20%	0806
R1, R2	Dependent on bus speed and parasitic capacitances	Optional pull-up resistors for TWI, 0.05 W, ±1%	0201
R3, R4	See Output voltage selection on page 41	Resistors for setting the BUCK1 and BUCK2 output voltages, 0.05 W, ±1%	0201
U1	nPM1300	nPM1300	QFN32 or WLCSP35

Table 37: Bill of material

9.3.2 Configuration 2

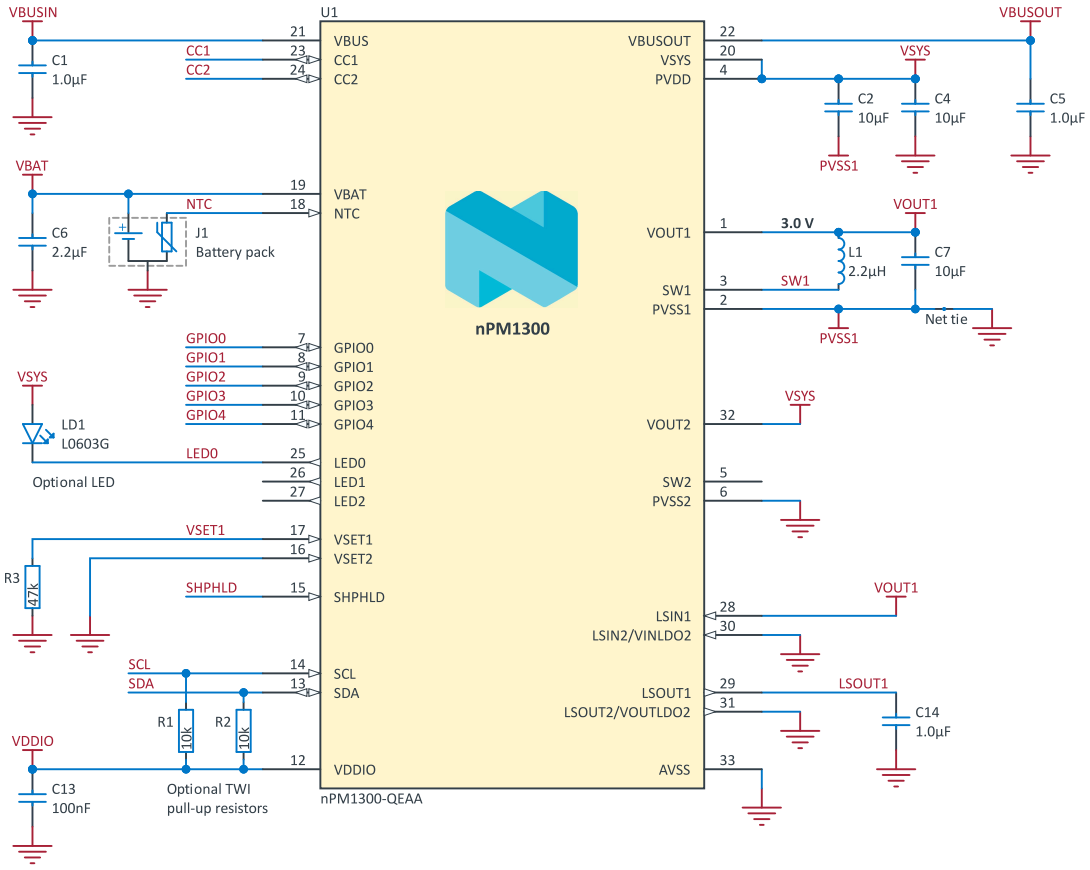

Figure 26: QFN schematic

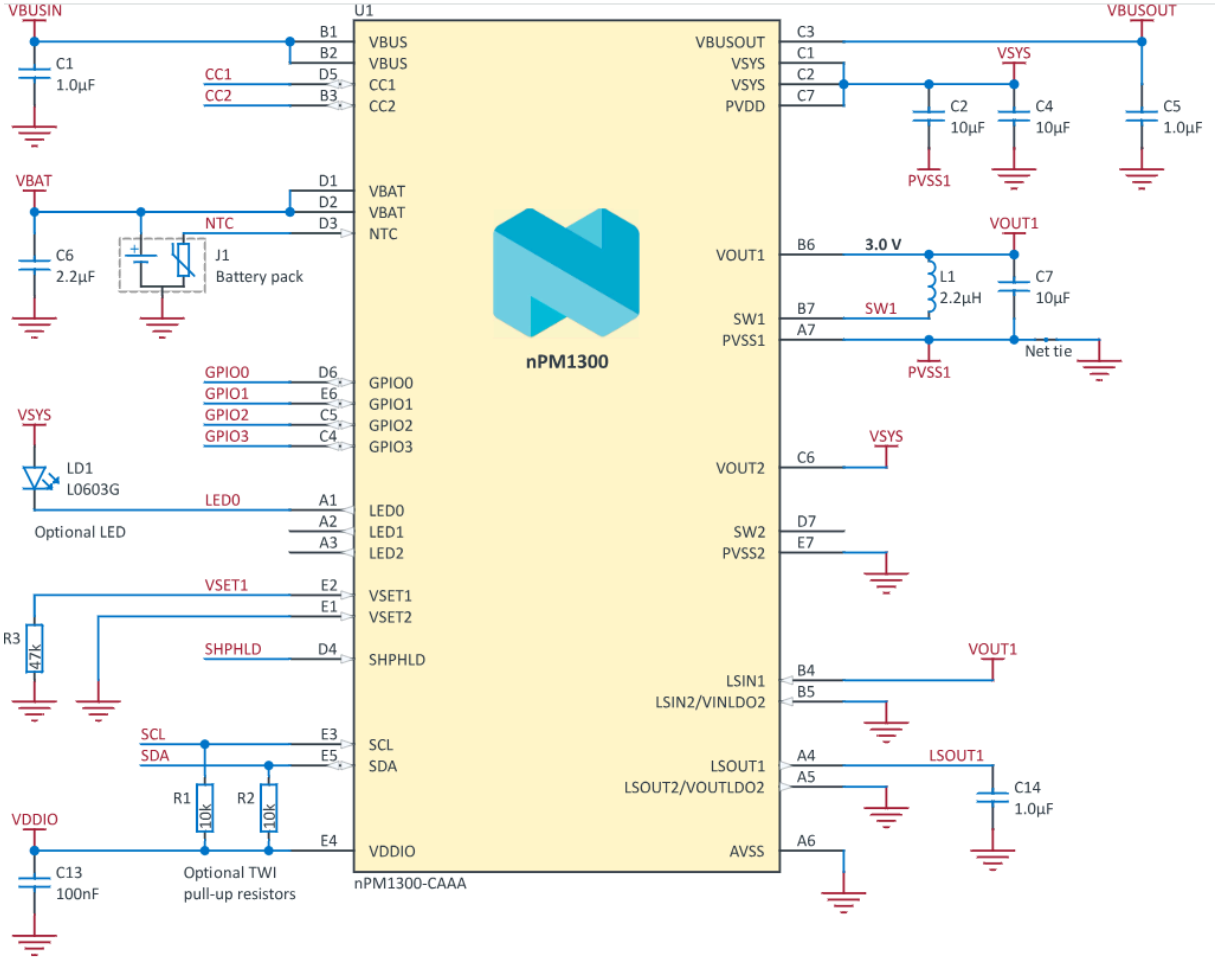

Figure 27: WLCSP schematic

Designator	Value	Description	Footprint
C1, C5, C14	1.0 µF	Capacitor, X5R, 10 V, ±10%	0603
C2, C4, C7	10 µF	Capacitor, X5R, 25 V, ±20%	0603
C6	2.2 µF	Capacitor, X5R, 25 V, ±10%	0603
C13	100 nF	Capacitor, X5R, 25 V, ±10%	0201
L1	2.2 µH	Inductor, DCR < 400 mΩ, ±20%	0806
R1, R2	Dependent on bus speed and parasitic capacitances	Optional pull-up resistors for TWI, 0.05 W, ±1%	0201
R3	See Output voltage selection on page 41	Resistors for setting the BUCK1 and BUCK2 output voltages, 0.05 W, ±1%	0201
U1	nPM1300	nPM1300	QFN32 or WLCSP35

Table 38: Bill of material

9.3.3 Configuration 3

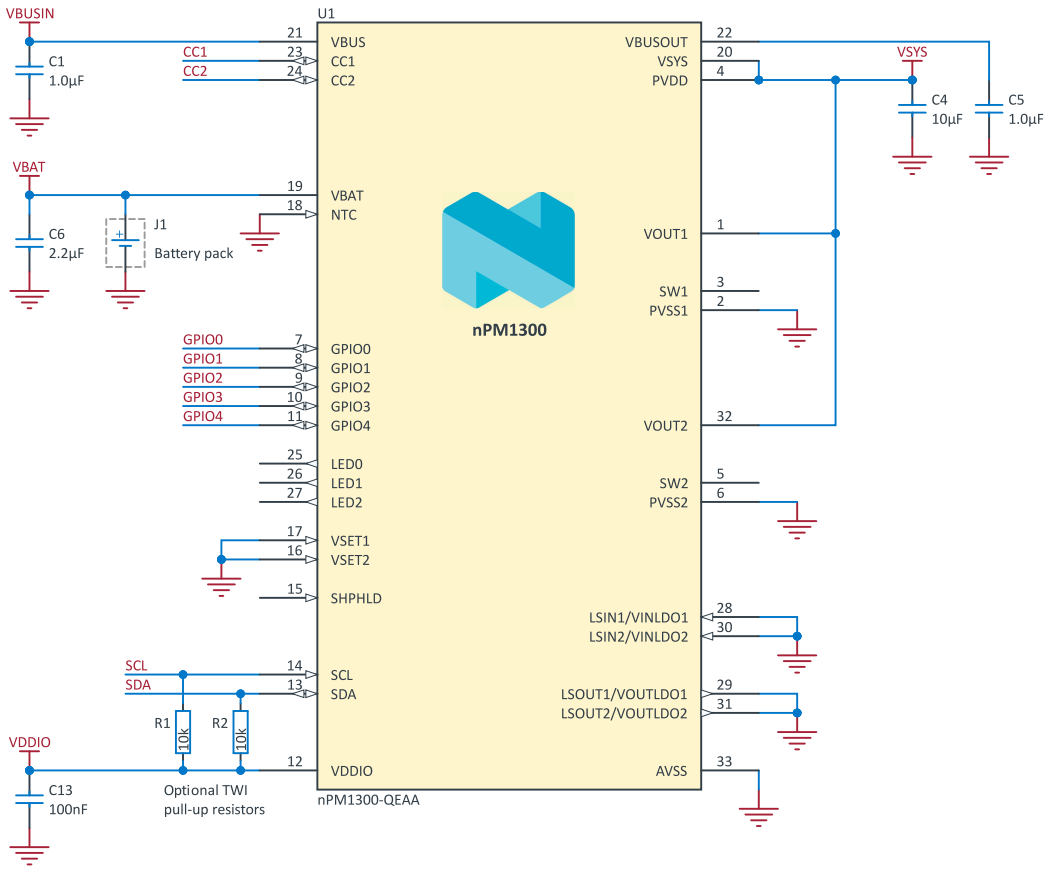

Figure 28: QFN schematic

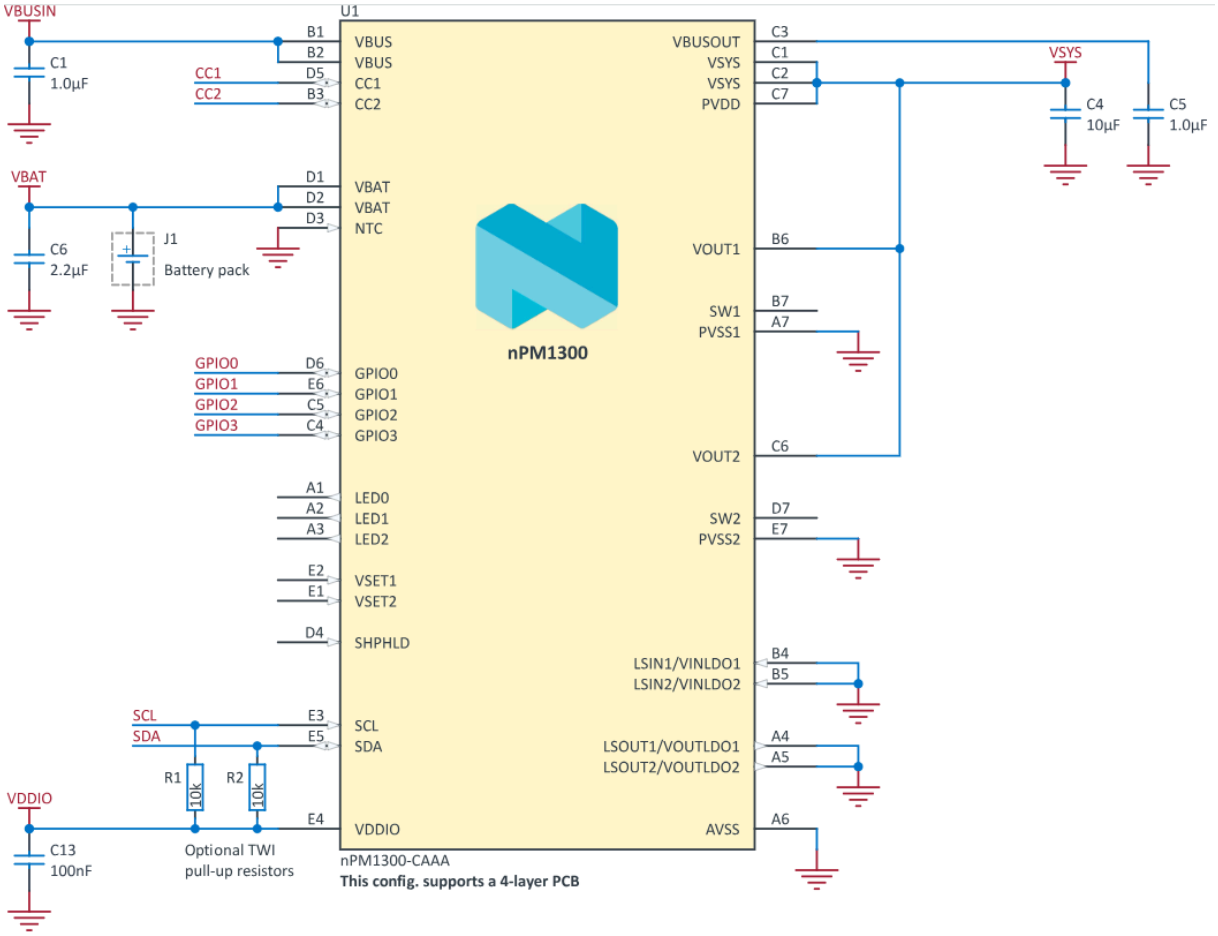

Figure 29: WLCSP schematic

Designator	Value	Description	Footprint
C1, C5	1.0 µF	Capacitor, X5R, 10 V, ±10%	0603
C4	10 µF	Capacitor, X5R, 25 V, ±20%	0603
C6	2.2 µF	Capacitor, X7R, 16 V, ±10%	0603
C13	100 nF	Capacitor, X5R, ±10%	0201
R1, R2	Dependent on bus speed and parasitic capacitances	Optional pull-up resistors for TWI, 0.05 W, ±1%	0201
U1	nPM1300	nPM1300	QFN32 or WLCSP35

Table 39: Bill of material

9.3.4 PCB guidelines

A well designed PCB is necessary to achieve good performance. A poor layout can lead to loss in performance or functionality.

To ensure functionality, it is essential to follow the schematics and layout references closely.

A PCB with a minimum of two layers, including a ground plane, is recommended for optimal performance.

The BUCK supply voltage should be decoupled with high performance capacitors as close as possible to the supply pins.

Long power supply lines on the PCB should be avoided. All device grounds, VDD connections, and VDD bypass capacitors must be connected as close as possible to the device.

9.3.5 PCB layout example

The PCB layouts are shown here for QFN followed by WLCSP.

QFN PCB layout

For all available reference layouts, see the Reference Layout section on the Downloads tab for nPM1300 on www.nordicsemi.com.

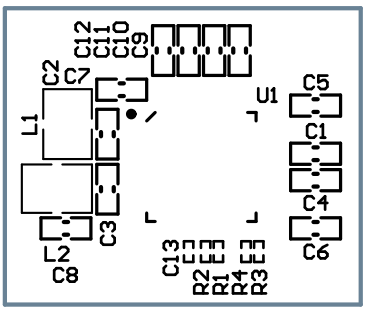

Figure 30: Top silkscreen layer QFN

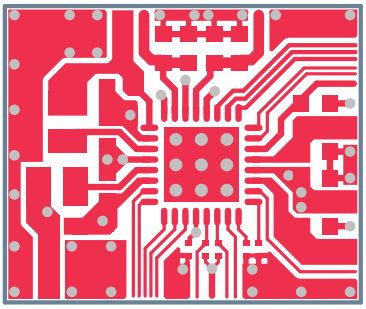

Figure 31: Top layer QFN

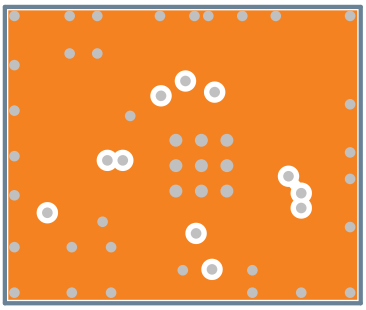

Figure 32: Mid layer 1 QFN

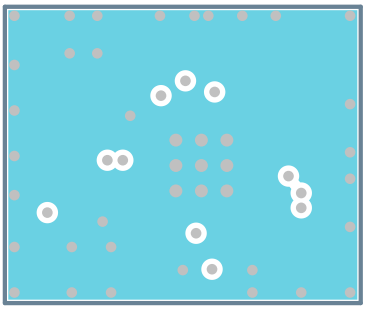

Figure 33: Mid layer 2 QFN

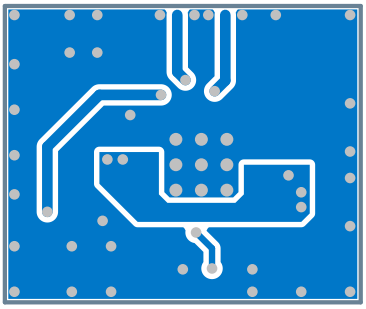

Figure 34: Bottom layer QFN

Note: No components on the bottom layer.

WLCSP PCB layout

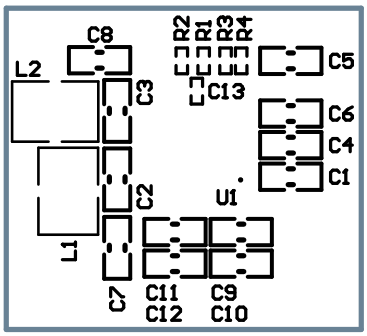

Figure 35: Top silkscreen layer WLCSP

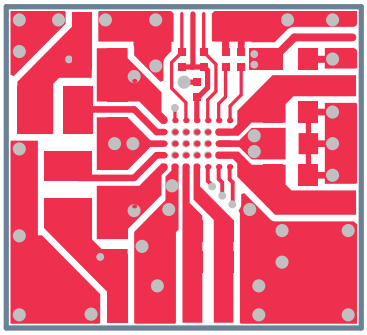

Figure 36: Top layer WLCSP

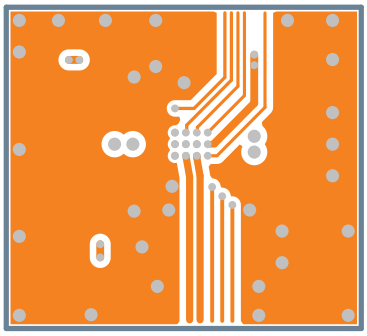

Figure 37: Mid layer 1 WLCSP

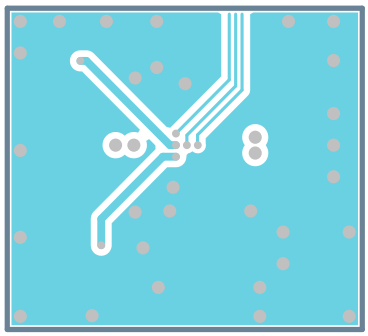

Figure 38: Mid layer 2 WLCSP

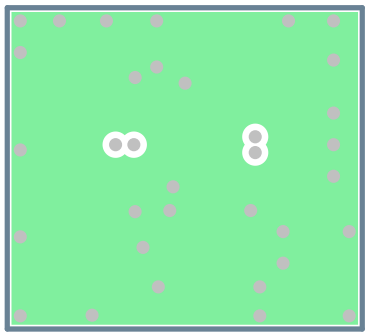

Figure 39: Mid layer 2 WLCSP

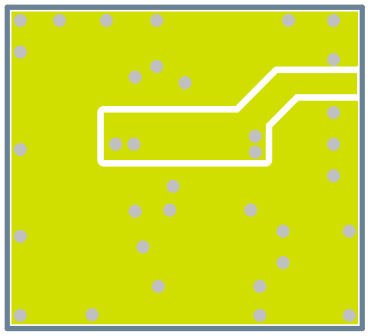

Figure 40: Mid layer 4 WLCSP

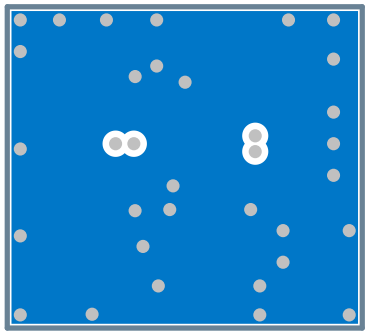

Figure 41: Bottom layer WLCSP

Note: No components on the bottom layer.

10 Ordering information

This chapter contains information on IC marking, ordering codes, and container sizes.

10.1 IC marking

The nPM1300 PMIC package is marked as shown in the following figure.

N	P	M	1	3	0	0
<P	P>	<V	V>	<H>	<P>	
<Y	Y>	<W	W>	<L	L>	

Figure 42: IC marking

10.2 Box labels

The following figures define the box labels used for nPM1300.

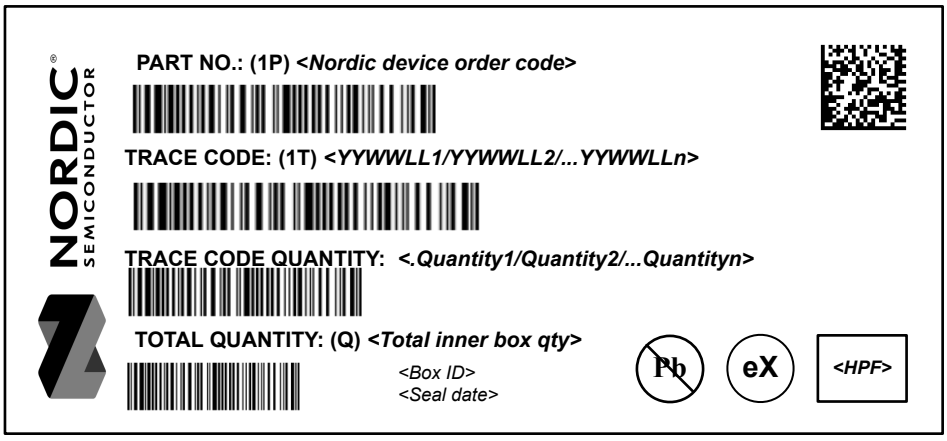

Figure 43: Inner box label

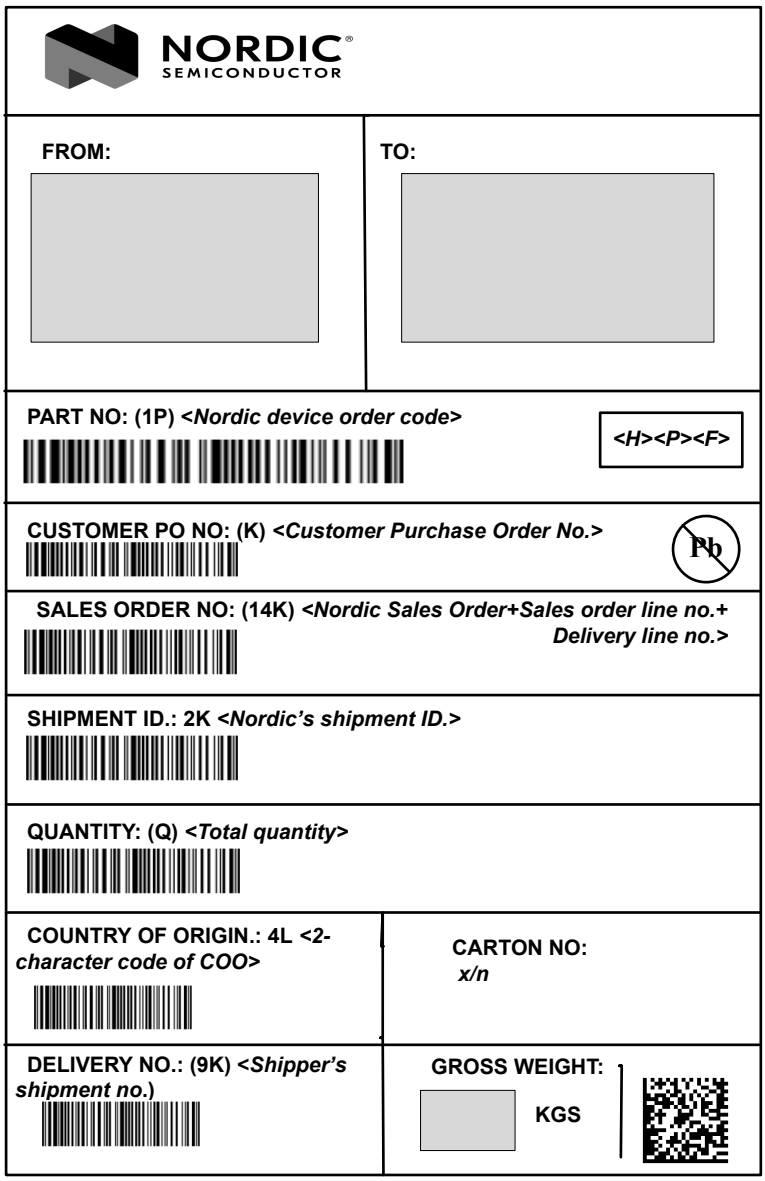

Figure 44: Outer box label

10.3 Order code

The following tables define nPM1300 order codes and definitions.

n	P	M	1	3	0	0	-	<P	P>	<V	V>	-	<C	C>

Figure 45: Order code

Abbreviation	Definition and implemented codes
nPM13	nPM13 series product
00	Part code
<PP>	Package variant code
<VV>	Function variant code
<H><P><F>	Build code H - Hardware version code P - Production configuration code (production site, etc.) F - Firmware version code (only visible on shipping container label)
<YY><WW><LL>	Tracking code YY - Year code WW - Assembly week number LL - Wafer lot code
<CC>	Container code
eX	2nd level Interconnect Symbol where value of X is based on J-STD-609

Table 40: Abbreviations

10.4 Code ranges and values

The following tables define the nPM1300 code ranges and values.

<PP>	Package	Size (mm)	Pin/Ball count	Pitch (mm)
CA	WLCSP	3.1x2.4	35	0.419 0.440
QE	QFN	5.0x5.0	32	0.5

Table 41: Package variant codes

<VV>	Flash (kB)	RAM (kB)
AA	n/a	n/a

Table 42: Function variant codes

<H>	Description
[A . . Z]	Hardware version/revision identifier (incremental)

Table 43: Hardware version codes

<P>	Description
[0 . . 9]	Production device identifier (incremental)
[A . . Z]	Engineering device identifier (incremental)

Table 44: Production configuration codes

<F>	Description
[A . . N, P . . Z]	Version of preprogrammed firmware
[0]	Delivered without preprogrammed firmware

Table 45: Production version codes

<YY>	Description
[16 . . 99]	Production year: 2016 to 2099

Table 46: Year codes

<WW>	Description
[1 . . 52]	Week of production

Table 47: Week codes

<LL>	Description
[AA . . ZZ]	Wafer production lot identifier

Table 48: Lot codes

<CC>	Description
R7	7" Reel
R	13" Reel

Table 49: Container codes

10.5 Product options

The following tables define nPM1300 product options.

Order code	MOQ[1]	Comment
nPM1300-CAAA-R	7000 pcs	Availability to be announced
nPM1300-CAAA-R7	1500 pcs	
nPM1300-QEAA-R	7000 pcs	
nPM1300-QEAA-R7	1500 pcs	

Table 50: nPM1300 order codes

Order code	Description
nPM1300-EK	Evaluation kit

Table 51: Development tools order code

[1] Minimum Ordering Quantity

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